MB55 IDTV
SERVICE MANUAL

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1. INTRODUCTION

17MB55 main board is driven by Novatek NT72568. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS/mini-LVDS transmitting, channel and MPEG2/4 decoding, integrated DVB-T/C demodulators and media center functionality.

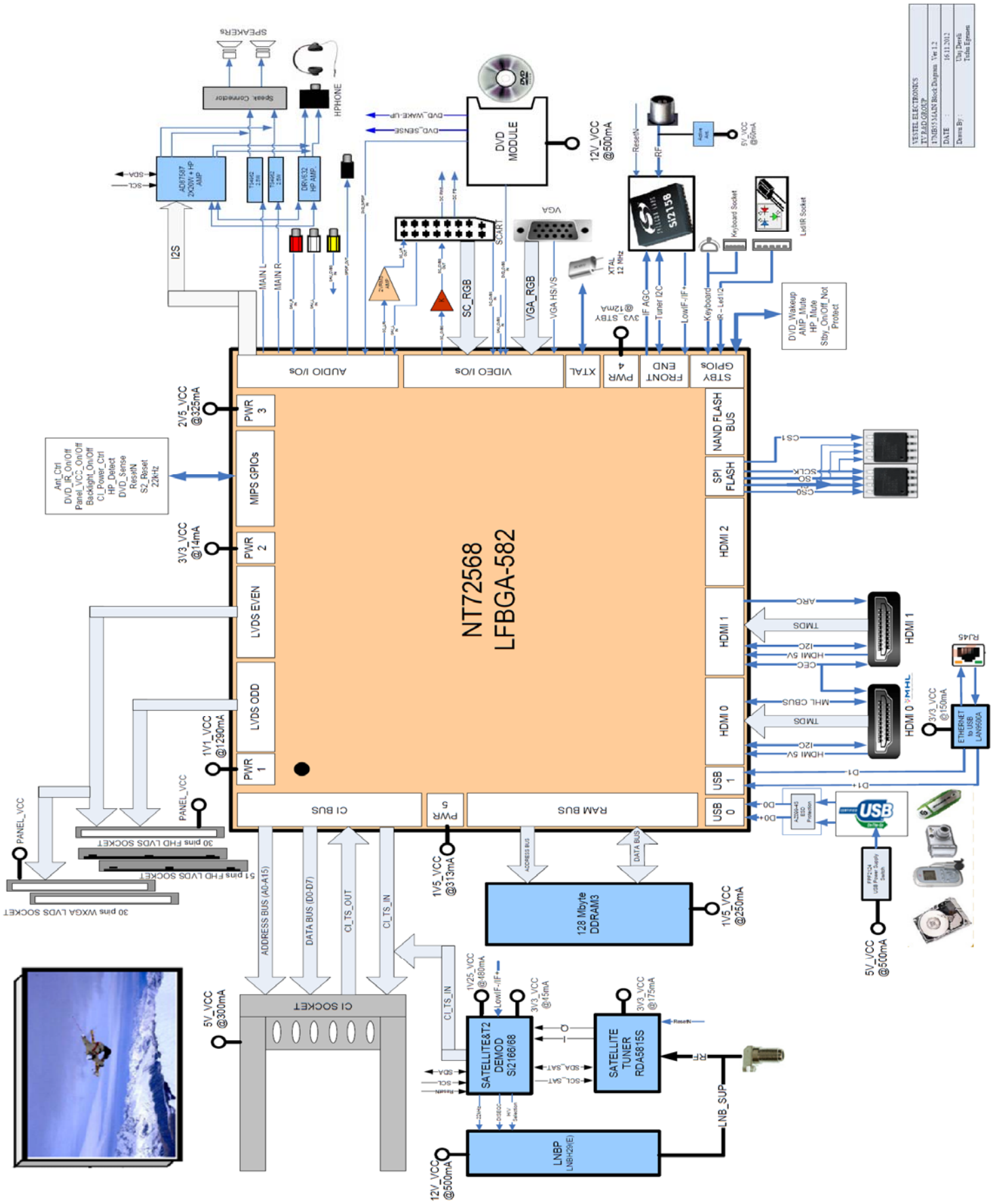
TV supports PAL, SECAM, NTSC color standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C is supported internal demodulators of Novatek IC and DVB-S/S2 and DVB-T2 are supported with external demodulator.

Sound system output is supplying maximum 2X8W (less 10%THD at max output) for stereo 8Ω speakers. Also there are 2 more audio power options, 2X6W @8 Ω and 2X2.5W @4 Ω

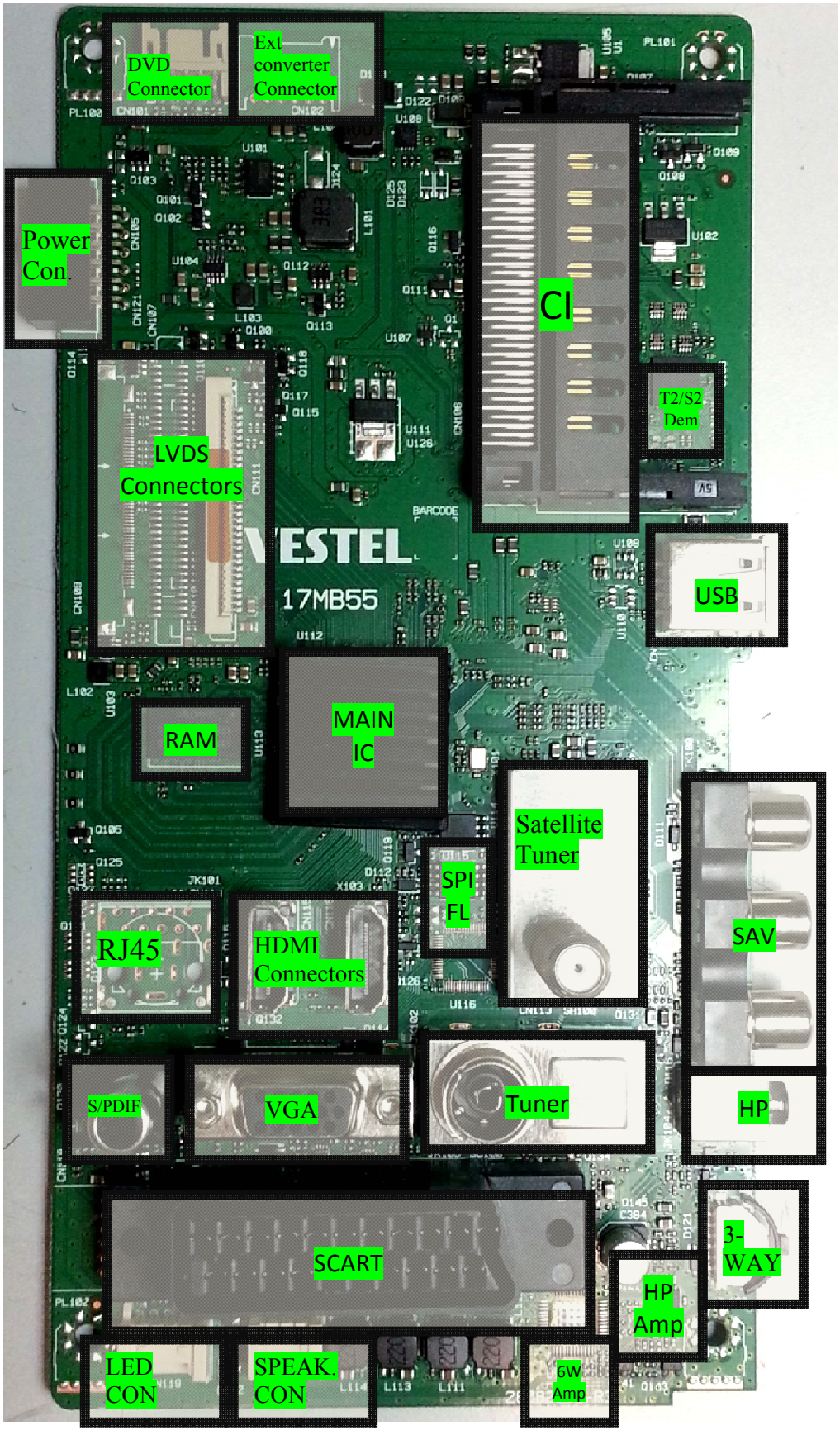
Supported peripherals are;

- 1 RF input VHF I, VHF III, UHF @ 75Ohm (Common)
- 1 Sat RF input @ 75Ohm (Optional)
- 1 Side AV (CVBS, R/L Audio) (Common)
- 1 SCART socket (Common)
- 1 PC input (Common)
- 2 HDMI 1.3 input (1 HDMI input is common, 1 input is optional)
- 1 S/PDIF output (Optional)
- 1 Headphone (Common)
- 1 Common Interface (Common)
- 1 USB (Common)
- 1 On-board Keypad (Optional)
- 1 External keypad Touchpad/Tact switch (Optional)

A. *GENERAL BLOCK DIAGRAM*



B. *PLACEMENT OF BLOCKS*



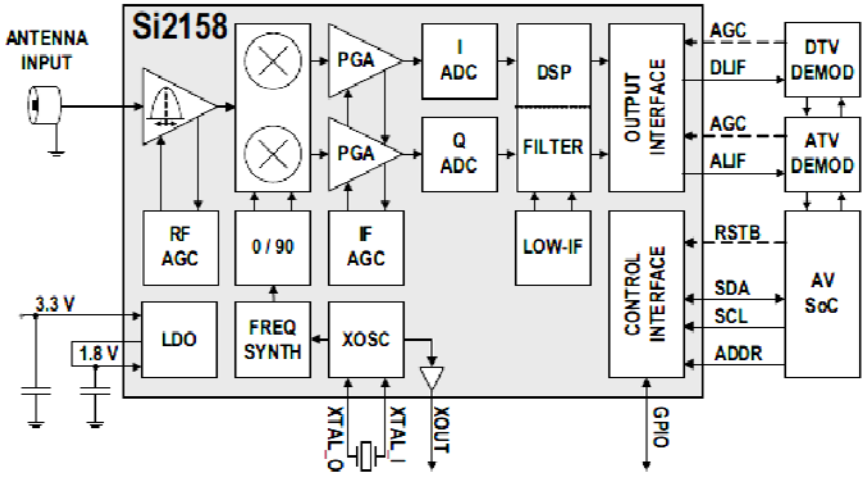
2. T/T2/C/A TUNER (U119)

The Si2158 is Silicon Labs' fourth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wire wound inductors or LNAs, the Si2158 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2158 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners and discrete MOPLL-based tuners. The Si2158 also incorporates a harmonic-rejection mixer to deliver excellent Wi-Fi and LTE immunity. For the best performance with next-generation digital TV standards such as DVB-T2/C2, the Si2158 delivers industry-leading phase noise performance.

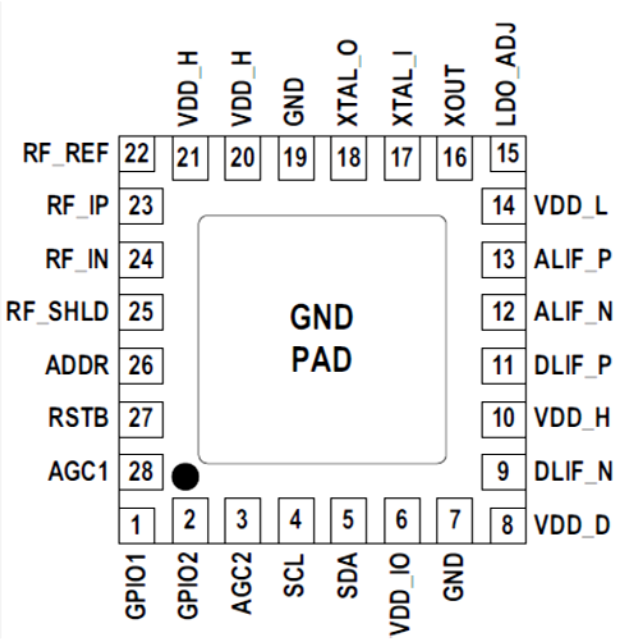
Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
  - 42-1002 MHz frequency range
- Industry-leading margin to A/74,NorDig, DTG, ARIB, EN55020,OpenCable™
- Lowest BOM for a hybrid TV tuner
  - No balun at RF input
  - Integrated tracking filters requiring no external inductors or SAW filters
  - Increased ESD protection on 6 pins
- Best-in-class real-world reception
  - Exceeds MOPLL-based tuners
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - 3.3 V single-supply option
- Integrated power-on reset circuit
- Single or separate output pins for ALIF/DLIF connection to SoC
- Standard CMOS process
- 4 x 4 mm, 28-pin QFN package
- RoHS compliant

Block Diagram



Pinning



3. S/S2 TUNER (U125) OPTIONAL

The RDA5815s is a fully integrated direct conversion RF front end for DVB-S,DVB-S2&ABS-S,MMDS digital satellite Reception standard CMOS process. The receiving frequency range is from 250MHz to 2150MHz, and the baseband filter's bandwidth can be selected from 4MHz to 40MHz with 1MHz step.

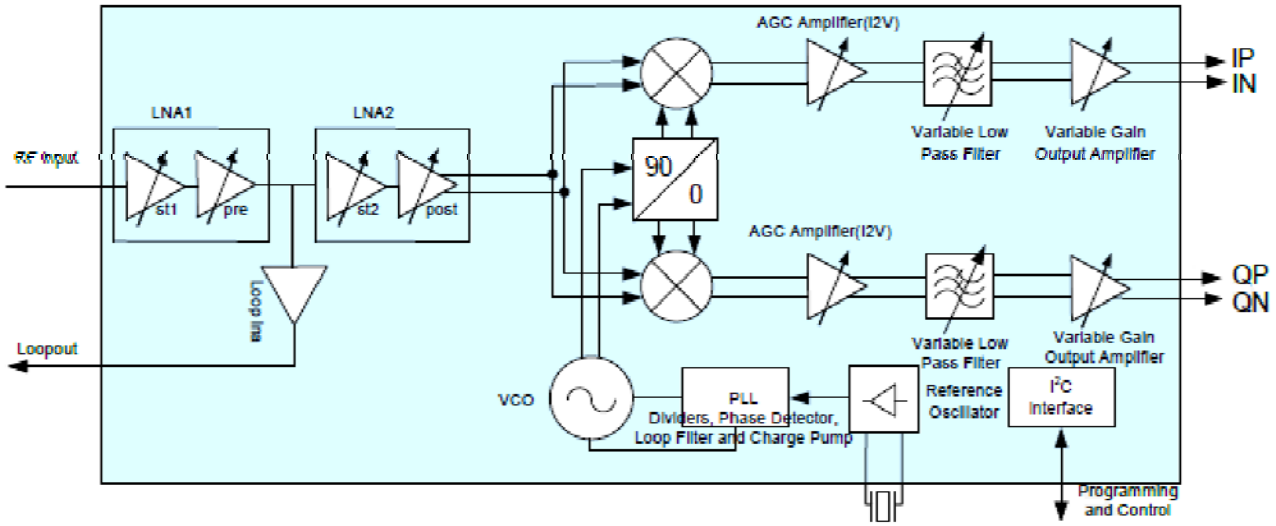
The RDA5815s consists of a variable gain LNA, quadrature down converter, variable IF gain amplifiers, variable low-pass filters, reference oscillator, VCOs, synthesizer and output baseband amplifier to drive external ADC.

Based on RDA's some innovative technique, the rda5815s offers excellent phase noise and very low implementation loss, required for advanced modulation systems such as 8PSK and DVB-S2. This tuner RF IC does not require a balun and its fully integrated design saves valuable board space and simplifies RF layout.

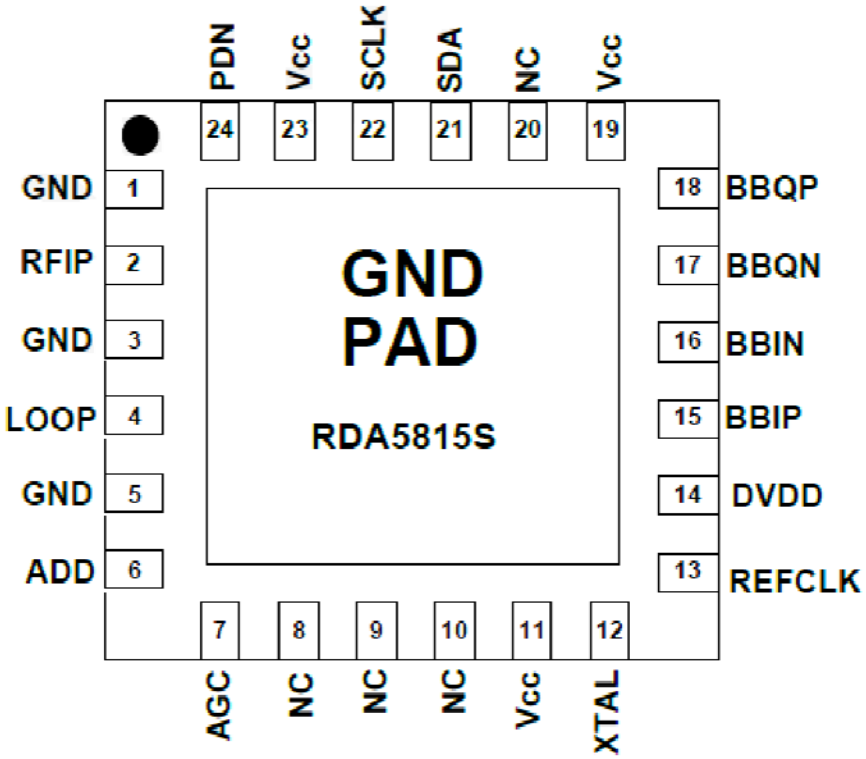
Features

- Single-Chip RF to baseband Satellite receiver
- CMOS Fully integrated RF front end
- Low noise and wide dynamic range zero IF receiver
- Input frequency range:250 to 2150 MHz
- Input signal level: -100 to 5dBm
- More than 85dB gain control range
- Fully integrated PLL
- Integrated RX VCO
- Integrated baseband LPF with selectable cut-off frequency from 4Mhz to 40Mhz with 1Mhz step
- Integrated LNA with RF AGC
- Integrated reference oscillator
- I2C bus interface
- Automatic gain control
- 0.11um RF CMOS technology
- 3V to 3.6V operations
- Power consumption of less than 600mW
- Lower profile packages 4X4mm QFN24

Block Diagram



Pinning



4. T2 or S/S2 DEMODULATOR (U106) OPTIONAL

The Si216X family has 3 different IC which are pin to pin compatible. DVB-S/S2 is supported by Si2166 and DVB-T2 is supported by Si2168.

Silicon Labs' DVB-T2 demodulator can accept a standard IF (36 MHz) or low-IF input and supports all modes specified by current DVB-T2 standard. The main features of the DVB-T2 mode are 256 QAM with rotated constellations, SISO and MISO support, FEF management, fully autonomous signal acquisition including automatic L1 signaling parsing, 600 kHz acquisition range, support for all pilot patterns, and DVB-T2/T auto-detection. Optimized DVB-T2 timing acquisition locks in less than 1 second under all echo conditions specified in Nordig 2.2.1. Silicon Labs' innovative LDPC and BCH decoding architecture delivers best-in-class performance for DVB-T2 and DVB-S2 broadcast reception while limiting the size and power consumption of the device. Moreover, the Si2169 uses only two power supplies: 1.2 and 3.3 V.

The satellite demodulation functionality allows demodulating widespread DVB-S, DIRECTV™ (DSS) legacy standards, and new generation DVB-S2 and DIRECTV™ (AMC) satellite broadcasts. A zero-IF interface allows for a seamless connection to market proven satellite silicon tuners. Constant coding modulation (CCM), 64800 bits frame, and a single TS, broadcast profile, are the main specifications of the DVB-S2 demodulator. It also integrates DiSEqC™ 2.0 LNB interface for satellite dish control and an equalizer to compensate for echoes in long cable feeds from the LNB to the satellite tuner RF input.

The Si2169 offers an on-chip blind scanning algorithm for DVB-S/S2 and DVB-C standards, as well as a blind lock subset mode. The DVB-T and DVB-C demodulators leverage field-proven technology of Silicon Labs' Si2161/63/65/67 family of digital television demodulators.

An I^2C host bus interface is used to configure the device via high-level API Commands. An internal pass-through switch acts as an I^2C repeater in order to transfer I^2C commands to the tuner and to provide a "quiet" I^2C bus to the RF front-end. The Si2169 contains an on-chip crystal oscillator and only requires the connection of a standard crystal or a reference clock. Crystal frequencies between 16 and 30 MHz are supported. Alternatively, a clock signal from 4 to 30 MHz (as available, for example, from the tuner) can be connected to the device's clock input, eliminating the need for a dedicated crystal. Additionally, four flexible multipurpose pins can carry AGC signals to the tuners, tuner AGC freeze signal for FEF and logic or PWM modulated signals.

The Si2169 programmable transport stream interface provides a flexible range of output modes (serial, master parallel, and slave parallel modes) and is fully compatible with all MPEG decoders or conditional access modules to support any customer application. It also embeds memory buffering for de-jittering purposes. In master parallel mode, the TS clock can be set with a constant period. Furthermore, a TS slave parallel mode is available in which the device indicates the availability of TS data in its internal output FIFO to a host, which then reads out this data.

The Si2169 guarantees a low-cost system implementation due to its minimal bill of materials and PCB footprint. A maximum of 24 components (R, C, and crystal, depending on the application selected) and only 20 by 20 mm on a 2-layer PCB are required. The new Si2169 and the former Si2167 (multimedia demodulator for DVB-T/C/S/S2) are pin-to-pin and power supply compatible on the PCB

Features

Common Features:

- DSP-based synchronization and demodulation control
  - Embedded ROM/NVM-coded firmware avoids code download and allows immediate operation at startup
  - Supports firmware patch code downloads for in-field upgradeability
- Lock, BER, PER, and SNR indicators
- Fast scanning functionality for all media, including efficient blind scan for satellite and cable
- 12-bit ADCs with independent IF and ZIF inputs for terrestrial/cable and satellite respectively (1 Vpp differential inputs)
- Power consumption: <550 mW in DVB-S2 modes; <450 mW in DVB-T2 modes; <200 mW in DVB-T and DVB-C modes
- Automatic spectral inversion detection for all media
- Clocks derived from 16–30 MHz crystal using an on-chip oscillator or by connection to 4–30 MHz tuner reference clock.
- Clock output to drive a secondary demodulator
- Up to 4 multipurpose ports to control tuners' AGC, and tuner AGC freeze
- Two GPIOs
- Master TS output modes, parallel or serial (with tri-state function)
- Slave TS parallel output interfaces seamlessly to external controllers for USB2.0, PCI-E, etc. External device polls data from on-chip FIFO via GPIF interface
- I^2C serial bus interfaces (master and host)
- 3.3 and 1.2 V power supplies
- Minimal BOM using standard components
- Ultra-compact QFN-48, 7x7 mm, Pb-free/RoHS-compliant package
- Pin-to-pin compatible with Si2166-B/67-B and Si2168

For DVB-T2:

- Bandwidth: 1.7, 5, 6, 7 or 8 MHz (and extended bandwidth)
- DVB-T2 versus DVB-T automatic detection
- Carrier recovery: ±600 kHz
- Timing recovery: ±200 ppm
- Supports all DVB-T2 modulation parameters:
  - All guard intervals, all FFT including extended bandwidth, all pilot patterns,
  - All rotated and not-rotated constellations, all code rates and frame sizes.
- Accepts up to 255 PLP(s) and outputs the data PLP + the common PLP on a single TS
- FEF management with available output signal to freeze tuner AGC during FEF
- Advanced terrestrial channel equalizer
- State-of-the-art impulsive noise protection algorithm
- CPE compensation to counteract tuner phase noise

For DVB-T:

- Bandwidth: 6, 7, 8 MHz. ACI filtering for 7 MHz channels enables use of a fixed 8 MHz IF filter
- Carrier recovery: ±600 kHz
- Timing recovery: ±200 ppm
- Advanced terrestrial channel equalizer
- State-of-the-art impulsive noise protection algorithm
- CPE compensation to counteract tuner phase noise

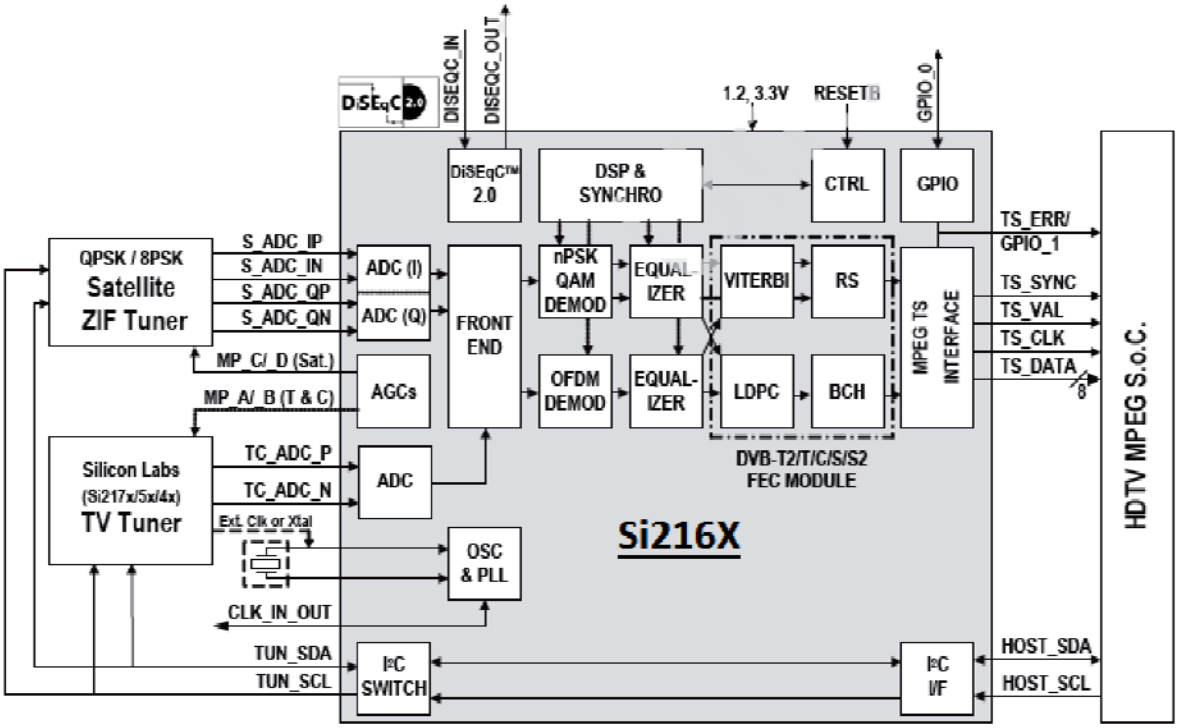
For DVB-C:

- DFE equalizer specific for cable network
- Carrier recovery: ± 11% of Symbol rate
- Timing recovery: ±1000 ppm

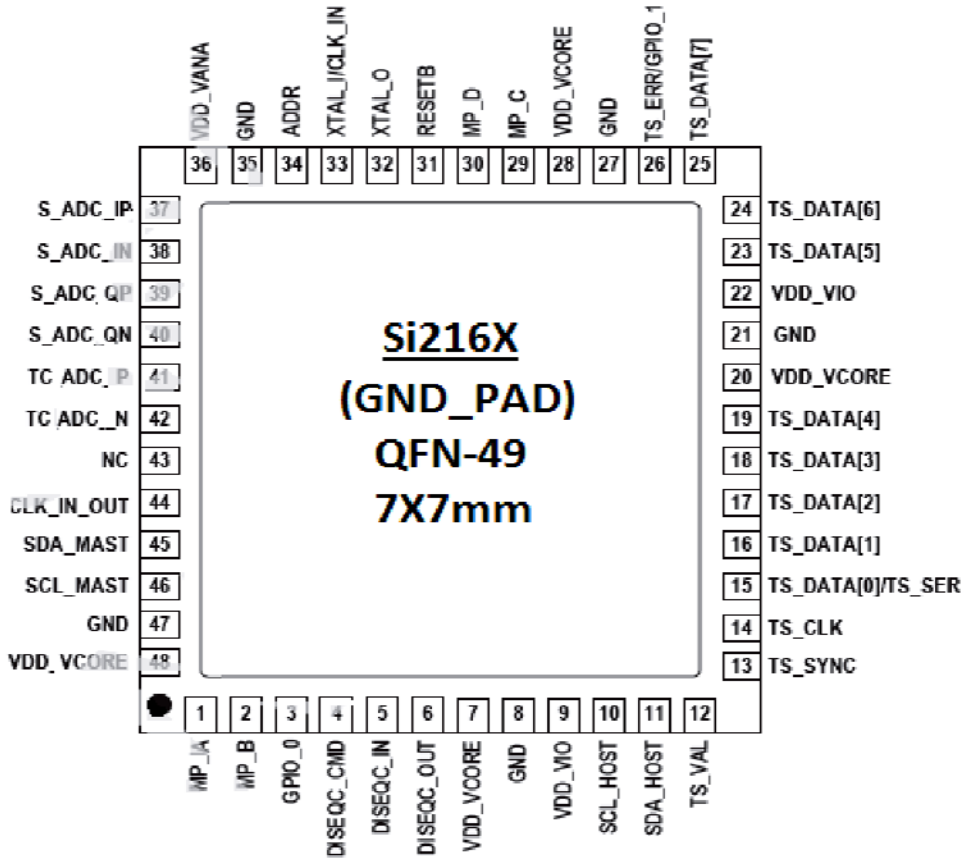
For DVB-S/S2:

- Programmable carrier recovery range
- Timing recovery: ±1000 ppm

Block Diagram



Pinning



5. LNB SUPPLY and CONTROL IC (U108) WITH SAT OPTIONAL

Intended for analog and digital satellite receivers/Sat-TV and Sat-PC cards, the LNBH29 series is a monolithic voltage regulator and interface IC, assembled in QFN16 (3x3) and QFN16 (4x4) specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with a simple design and I²C standard interfacing.

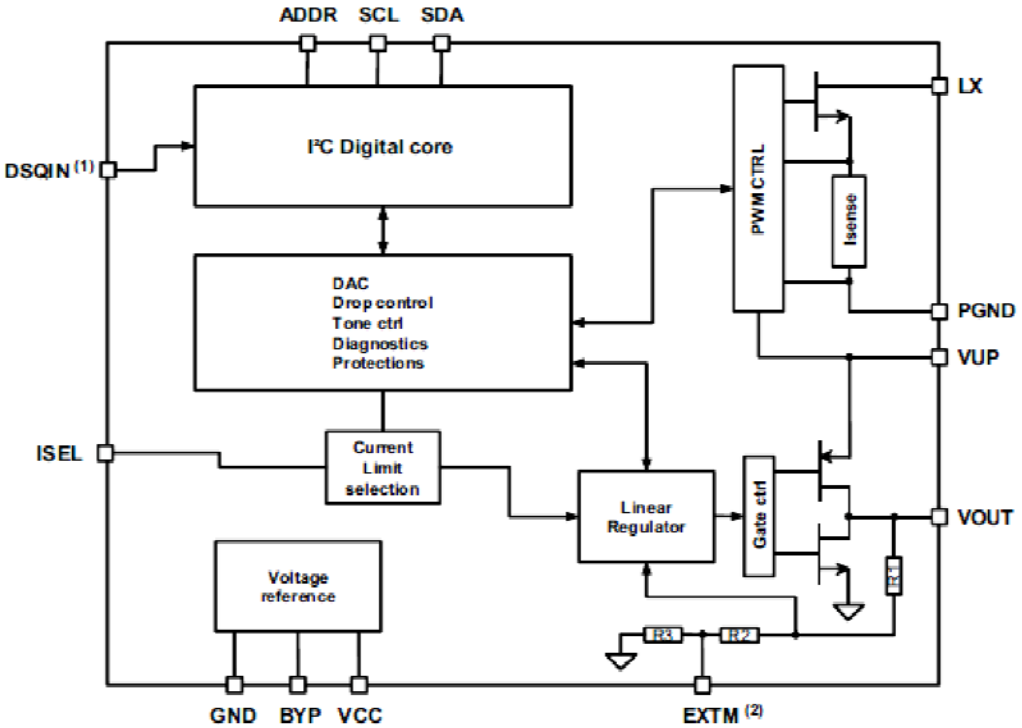
This IC has a built-in DC-DC step-up converter that, from a single source from 9 V to 17.5 V, generates the voltages (VUP) that allow the linear post-regulator to work with a minimum.

Dissipated power of 0.5 W typ. @ 500 mA load (the linear post-regulator drop voltage is internally kept at VUP - VOUT = 1 V typ.). The IC is also provided with an under voltage lockout circuit that disables the whole circuit when the supplied VCC drops below a fixed threshold (4.7 V typically). The step-up converter is provided with a soft-start function which reduces the inrush current during startup. The SS time is internally fixed at 4 ms typ. To switch from 0 to 13 V and 6 ms typ. to switch from 0 to 18 V.

Features

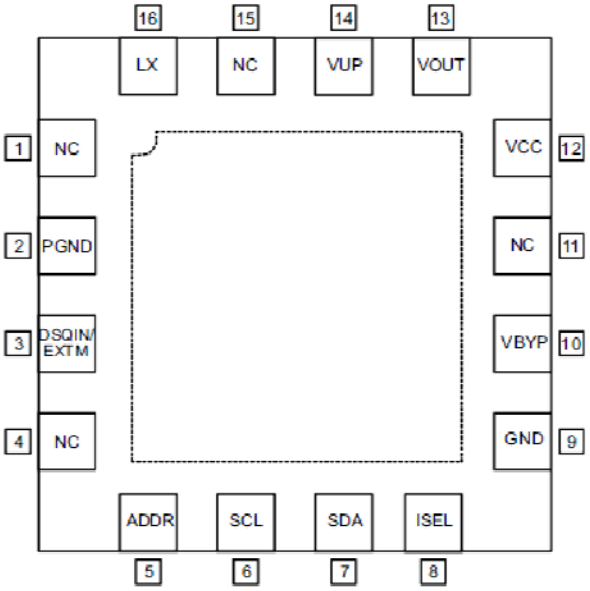
- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specifications
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- EXTM pin, auxiliary 22 kHz modulation input (LNBH29E) extends design flexibility
- 22 kHz tone waveform integrity guaranteed also at no load condition
- Low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allowing low power losses
- Overload and over temperature internal protection with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Block Diagram



Pinning

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pins voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
V_{EXTM}	EXTM pin voltage	-0.3 to 2	V
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) all pins, unless power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	



Pin n°	Symbol	Name	Pin function
16	LX	N-Mos drain	Integrated N-channel Power MOSFET drain.
2	P-GND	Power ground	DC-DC converter power ground. To be connected directly to the Epad.
5	ADDR	Address setting	Two I²C bus addresses available by setting the address pin level voltage.
6	SCL	Serial clock	Clock from I²C bus.
7	SDA	Serial data	Bi-directional data from/to I²C bus.
8	ISEL	Current selection	The resistor "RSEL" connected between ISEL and GND defines the linear regulator current limit threshold.
9	GND	Analog ground	Analog circuits ground. To be connected directly to the Epad.
10	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
12	V_{CC}	Supply input	8 to 17.5 V IC DC-DC power supply.
13	V_{OUT}	LNB output port	Output of the integrated very low drop linear regulator.
14	V_{UP}	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor.
3	DSQIN (LNBH29)	DiSEqC tone envelope input	Available for LNBH29 version: this pin accepts DiSEqC envelope codes (TTL compatible) from the main DiSEqC microcontroller. The LNBH29 uses this code to enable the internally generated 22 kHz carrier superimposed to the V_{OUT} pin DC voltage.
3	EXTM (LNBH29E)	External 22 kHz tone input	Available for LNBH29E version: the "external tone modulation" input acts on the integrated linear regulator loop to superimpose an external 22 kHz signal to the V_{OUT} pin DC voltage. Needs DC decoupling to the AC source.
Epad	Epad	Exposed pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.
1, 4, 11, 15	N.C.	Not internally connected	Not internally connected pins. These pins can be connected to GND to improve thermal performance.

6. AUDIO AMPLIFIER STAGE

A. AD87587 (U124) (OPTIONAL FOR 6W and 8W PRODUCTS)

The AD87587 is an integrated audio system solution, embedding digital audio process, power stage amplifier, and a stereo 2Vrms line driver, for driving stereo bridge-tied speakers and headphone. Using I2C digital control interface, the user can control AD87587's input format selection, mute and volume control functions. AD87587 has many built-in protection circuits to safeguard AD87587 from connection errors. It can provide 20W output power to stereo amplifiers or 40W output power for mono applications.

Features

- 16/18/20/24-bit input with I2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  32 kHz/ 44.1 kHz / 48 kHz and
  64 kHz/ 88.2 kHz / 96 kHz and
  128 kHz/176.4 kHz/192 kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  256x~1024x Fs for 32 kHz/ 44.1 kHz / 48 kHz
  128x~512x Fs for 64 kHz/ 88.2 kHz / 96 kHz
  64x~256x Fs for 128 kHz/176.4 kHz/192 kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  10W x 2ch into 8_ @ 0.16% THD+N
  15W x 2ch into 8_ @ 0.18% THD+N
  20W x 2ch into 8_ @ 0.24% THD+N
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate
  DC-blocking high-pass filter 1
- Anti-pop design
- Short circuit and over-temperature protection

- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Dynamic temperature control

Electrical Characteristics

General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{PD(VDDL/R)}$	VDDL/R Supply Current during Power Down	VDDL/R=24V		40	200	uA
$I_{PD(DVDD)}$	DVDD Supply Current during Power Down	DVDD=3.3V		4	20	uA
$I_{SD(PVDD)}$	PVDD Supply Current during Shutdown	PVDD=3.3V			100	uA
$I_{Q(VDDL/R)}$	Quiescent current for VDDL+VDDR (50%/50% PWM duty)	VDDL/R=24V		19		mA
$I_{Q(DVDD)}$	Quiescent current for DVDD	DVDD=3.3V		16.5		mA
$I_{Q(PVDD)}$	Quiescent current for PVDD	PVDD=3.3V		7	15	mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
UV_H	Under Voltage Disabled (For DVDD)			2.8		V
UV_L	Under Voltage Enabled (For DVDD)			2.7		V
Rds-on	Static Drain-to-Source On-state Resistor, PMOS	VDDL/R=24V, Id=500mA		260		mΩ
	Static Drain-to-Source On-state Resistor, NMOS			175		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	VDDL/R=24V		5		A
	Mono Channel Over-Circuit Protection (Note 2)	VDDL/R=24V		10		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
$I_{(EN)}$	EN pin Input Current	PVDD=3.3V		0.1		uA
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Electrical Characteristics and Specifications for Loudspeaker

- **Stereo output with 24V supply voltage**

Condition: T_A=25 °C, DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=8Ω with passive LC lowpass filter (L=22 μH with R_{DC}=0.12Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.21%)	+8dB volume			20		W
	RMS Output Power (THD+N=0.18%)				15		W
	RMS Output Power (THD+N=0.16%)				10		W
THD+N	Total Harmonic Distortion + Noise	P_O=7.5W			0.14		%
SNR	Signal to Noise Ratio (Note 8)	+8dB volume	-9dB		97		dB
DR	Dynamic Range (Note 8)	+8dB volume	-68dB		105		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			77		dB
	Channel Separation (non-shield choke)	P_O=1W at 1kHz			70		dB

Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

Electrical Characteristics and Specifications for Line Driver

- **Capless line driver**

PVDD=3.3V, T_A=25℃, R_L=2.5kΩ, C_{FLY}=C_{PVSS}=1μF, C_{IN}=1μF, R_I=10kΩ, R_F=20kΩ (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_O	Output Voltage (Outputs In Phase)	THD+N=1%, V_{DD}=3.3V, f_{IN}=1kHz		2.2		Vrms
THD+N	Total Harmonic Distortion Plus Noise	V_O=2Vrms, f_{IN}=1kHz		0.002		%
Crosstalk	Channel Separation	V_O=2Vrms, f_{IN}=1kHz		-106		dB
V_N	Output Noise	R_I=10k, R_F=10k		11	15	μVrms
V_{SR}	Slew Rate			8		V/μs
SNR	Signal to Noise Ratio	V_O=2Vrms, R_I=10k, R_F=10k, A-weighted		107		dB
G_{BW}	Unit-Gain Bandwidth			8		MHz
A_{VO}	Open-Loop Gain		80			dB
V_{OS}	Output Offset Voltage	V_{DD}=3V to 5.5V, Input Grounded	-5		5	mV
PSRR	Power Supply Rejection Ratio	V_{DD}=3V to 5.5V, V_{rr}=200mVrms, f_{IN}=1kHz		-80	-60	dB
R_I	Input Resistor Range		1	10	47	kΩ
R_F	Feedback Resistor Range		4.7	20	100	kΩ
f_{CP}	Charge-Pump Frequency		400	500	600	kHz
	Maximum capacitive Load			220		pF
V_{UVP}	External Under Voltage Detection			1.25		V
I_{HYS}	External Under Voltage Detection Hysteresis Current			5		μA
$T_{start-up}$	Start-up Time			0.5		ms

Absolute Maximum Ratings

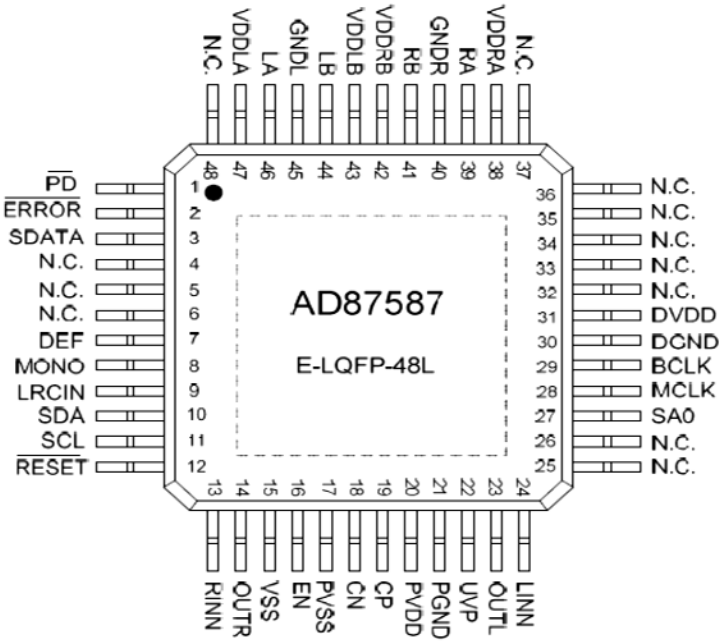
Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
PVDD	Supply for Line Driver	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_I	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
PVDD	Supply for Line Driver	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_a	Ambient Operating Temperature	0~70	°C

Pinning



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
2	$\overline{ERROR}$	O	Error status, low active	Open-drain output
3	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
4	N.C.			
5	N.C.			
6	N.C.			
7	DEF	I	Default volume setting	Schmitt trigger TTL input buffer
8	MONO	I	MONO mode enable, high active	Schmitt trigger TTL input buffer
9	LRCIR	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
10	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
11	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
12	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
13	RINN	I	Right input for line driver	
14	ROUT	O	Right output for line driver	
15	SGND	P	Ground for line driver	
16	EN	I	Enable for line driver	
17	PVSS	P	Supply voltage for line driver	
18	CN	I/O	Charge pump flying capacitor negative connection for line driver	
19	CP	I/O	Charge pump flying capacitor positive connection for line driver	
20	PVDD	P	Supply voltage for line driver	
21	PGND	P	Ground for line driver	
22	UVP	I	Under voltage protection for line driver	
23	LOUT	O	Left output for Line driver	
24	LINN	I	Left input for Line driver	
25	N.C.			
26	N.C.			
27	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
28	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
29	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
30	DGND	P	Digital Ground (3.3V)	
31	DVDD	P	Digital Power (3.3V)	
32	N.C.			
33	N.C.			
34	N.C.			
35	N.C.			
36	N.C.			
37	N.C.			
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.			

B. *TS4962M (U122 & U123) (OPTIONAL FOR 2.5W PRODUCTS)*

Features

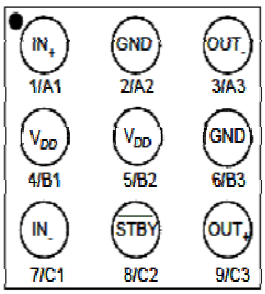
- Operating from V_{CC} = 2.4V to 5.5V
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300µm (Pb-free)

Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into a 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

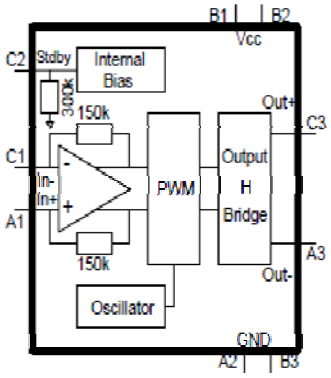
The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

Pin connections



IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output

Block diagram



C. DRV632 (U121) (OPTIONAL HP DRIVER FOR 2.5W PRODUCTS)

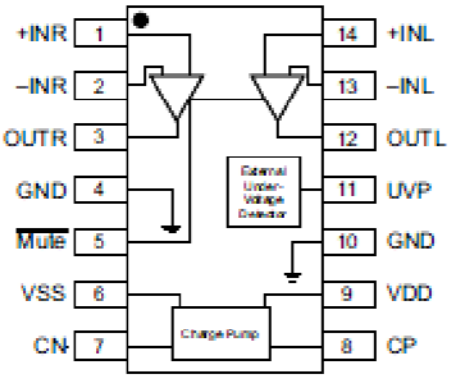
The DRV632 is a 2-VRMS pop-free stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single-supply electronics where size and cost are critical design parameters.

The DRV632 is capable of driving 2 VRMS into a 10-kΩ load with 3.3-V supply voltage. The device has differential inputs and uses external gain-setting resistors to support a gain range of ±1 V/V to ±10 V/V, and gain can be configured individually for each channel. The DRV632 has built-in active-mute control for pop-free audio on/off control. The DRV632 has an external under voltage detector that mutes the output when the power supply is removed, ensuring a pop-free shutdown.

The DRV632 does not require a power supply greater than 3.3 V to generate its 5.6-Vpp output, nor does it require a split-rail power supply. The DRV632 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased 2-VRMS output. The DRV632 is available in a 14-pin TSSOP.

Pin Description and Package View

PW PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN NAME	PIN NO.	I/O(1)	DESCRIPTION
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
Mute	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection; connect to PVDD with a 10-kΩ resistor if function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

Electrical and Operating Characteristics

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	VDD = 3.3 V		0.5	1	mV
PSRR	Power-supply rejection ratio			80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
V_{UVP_EX}	External UVP detect voltage			1.25		V
$V_{UVP\_EX\_HYSTERESIS}$	External UVP detect hysteresis current			5		µA
f_{CP}	Charge pump switching frequency		200	300	400	kHz
$\|I_{IH}\|$	High-level input current, $\overline{Mute}$	VDD = 3.3 V, V_{IH} = VDD			1	µA
$\|I_{IL}\|$	Low-level input current, $\overline{Mute}$	VDD = 3.3 V, V_{IL} = 0 V			1	µA
I_{DD}	Supply current	VDD = 3.3 V, no load, $\overline{Mute}$ = VDD	5	14	25	mA
		VDD = 3.3 V, no load, $\overline{Mute}$ = GND, disabled		14		

OPERATING CHARACTERISTICS

VDD = 3.3 V, R_{DL} = 10 kΩ, R_{FB} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_F = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, outputs in phase	THD+N = 1%, VDD = 3.3 V, f = 1 kHz, R_L = 10 kΩ	2	2.4		V_{rms}
THD+N	Total harmonic distortion plus noise	V_O = 2 V_{RMS}, f = 1 kHz		0.002%		
SNR	Signal-to-noise ratio(1)	A-weighted	90	105		dB
DNR	Dynamic range	A-weighted	90	105		dB
V_N	Noise voltage	A-weighted		11		µV
Z_O	Output impedance when muted	$\overline{Mute}$ = GND		110		mΩ
	Input-to-output attenuation when muted	$\overline{Mute}$ = GND		80		dB
	Crosstalk—L to R, R to L	V_O = 1 V_{rms}		–110		dB
I_{LIMIT}	Current limit			25		mA

(1) SNR is calculated relative to 2-Vrms output.

7. POWER STAGE

The DC voltages required for different blocks of the main board and panel are provided by main power supply unit. MB55 chassis can operate with PW05, IPS60, IPS61, IPS70, IPS20, IPS11, IPS16, IPS17, IPS19, PW25, PW26, PW03, PW04, PW06, and PW07 as main power supply and also with 12V adaptor. The main difference from previous projects MB55 uses the 2x6 pin power connector. And only 12V_STBY supply is necessary to provide all required board supplies. As the main power board has 2x6 pin option, MB55 can operate with above given power boards.

Which power board can be used for board to board or cable connection?

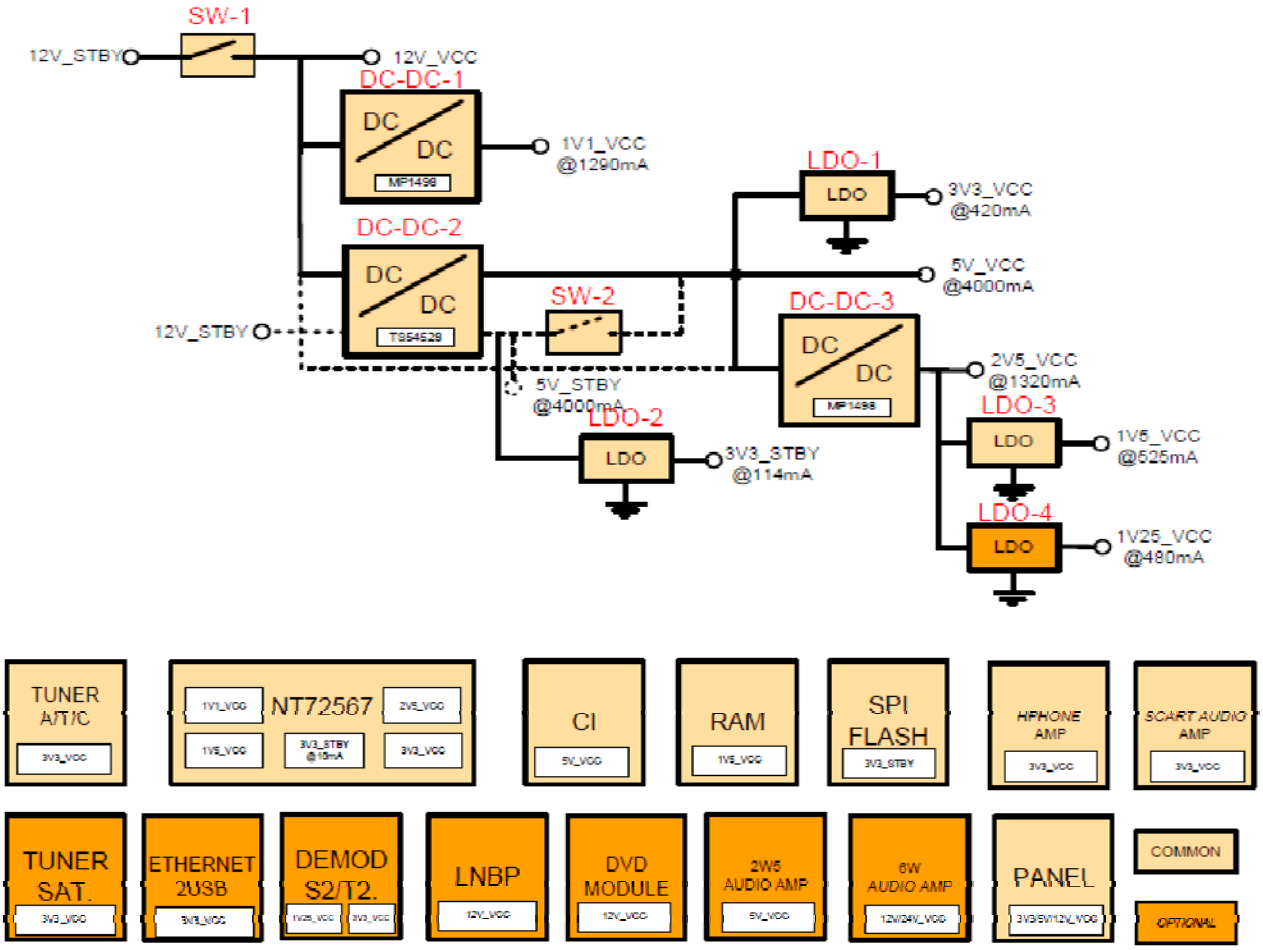
Board to board (BTB): PW05, IPS60, IPS61, IPS70, IPS11, IPS16, IPS17, IPS19

Power Cable: PW25, PW26, PW03, PW04, PW06, PW07, IPS20,

The power supplies generate 12V standby mode DC voltage and 24V system voltage only for audio IC voltage in necessary situations. Power stage which is on-chassis generates 5V, 3V3 stand by voltage and 12V, 5V, 3V3, 2.5V, 1.5V, 1.2 and 1.15V supplies for other blocks of the chassis. The power block diagram with the

blocks power requirements of MB55 is given below. And also you can find below the details about the Step down IC's and LDO's which are used in MB55 main board.

Power Management



A. RT7278 (U101) (3A) – RT7240 (U101) (5A)

The RT7278/RT7240 is a synchronous step down converter with Advanced Constant On-Time (ACOT) mode control. The ACOT provides a very fast transient response with few external components. The low impedance internal MOSFET supports high efficiency operation with wide input voltage range from 4.5V to 17V. The proprietary circuit of the RT7278/RT7240 enables to support all ceramic capacitors. The output voltage can be adjustable between 0.8V and 8V. The soft-start is adjustable by an external capacitor.

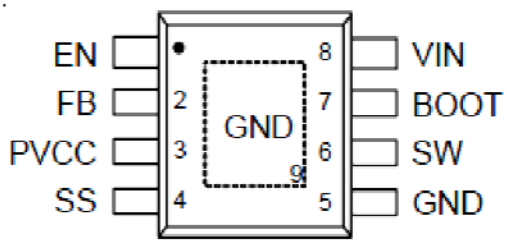
Features

- ACOT Mode Enables Fast Transient Response
- 4.5V to 17V Input Voltage Range
- 3A Output Current
- 60mOhm Internal Low Site N-MOSFET
- Advanced Constant On-Time Control
- Support All Ceramic Capacitors
- Up to 95% Efficiency

- 700kHz Switching Frequency
- Adjustable Output Voltage from 0.8V to 8V
- Adjustable Soft-Start
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- Thermal Shutdown Protection

Pinning

(TOP VIEW)



SOP-8 (Exposed Pad)

Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10L 3x3		
1	1	EN	Enable Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	2	FB	Feedback Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback reference voltage is 0.765V typically.
3	3	PVCC	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
4	4	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 1.5ms.
5, 9 (Exposed Pad)	5, 11 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	6, 7	SW	Switch Node. Connect this pin to an external L-C filter.
7	8	BOOT	Bootstrap for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	9, 10	VIN	Supply Input. The input voltage range is from 4.5V to 17V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	–	1.5	10	μA
Quiescent Current		I_Q	V_{EN} = 3V, V_{FB} = 1V	–	0.7	--	mA
Logic Threshold							
EN Voltage	Logic-High			2	--	17	V
	Logic-Low			–	--	0.4	
V_{REF} Voltage and Discharge Resistance							
Feedback Reference Voltage		V_{REF}	4.5V ≤ V_{IN} ≤ 17V	0.753	0.765	0.777	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	–0.1	0	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 17V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
Line Regulation			6V ≤ V_{IN} ≤ 17V, I_{PVCC} = 5mA	–	--	20	mV
Load Regulation			0 < I_{PVCC} < 5mA	–	--	100	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	–	110	--	mA
$R_{DS(ON)}$							
Switch On Resistance	High Side	$R_{DS(ON)\_H}$		–	90	--	mΩ
	Low Side	$R_{DS(ON)\_L}$		–	60	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
Current limit	I_{LIM}		3.5	4.1	5.7	A
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	
On-Time Timer Control						
On-Time	t_{ON}	V_{IN} = 12V, V_{OUT} = 1.05V	--	145	--	ns
Minimum On-Time	$t_{ON(MIN)}$		--	60	--	ns
Minimum Off-Time	$t_{OFF(MIN)}$		--	230	--	ns
Soft-Start						
SS Charge Current		V_{SS} = 0V	1.4	2	2.6	μA
SS Discharge Current		V_{SS} = 0.5V	0.1	0.2	--	mA
UVLO						
UVLO Threshold		VIN Rising to Wake up V_{PVCC}	3.55	3.85	4.15	V
Hysteresis			--	0.3	--	

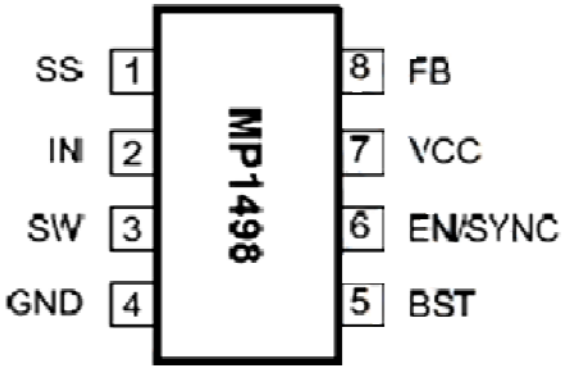
B. MP1498 (U103 & U104) (2A)

The MP1498 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs. It offers a very compact solution to achieve 2A continuous output current with excellent load and line regulation over a wide input supply range. The MP1498 has synchronous mode operation for higher efficiency over the output current load range. Current-mode operation provides a fast transient response and eases loop stabilization. Protective features include over-current protection, thermal shutdown, and external SS control.

Features

- Wide 4.5V-to-16V Operating Input Range
- 100mΩ/40mΩ Low RDS(ON) Internal Power MOSFETs
- Proprietary Switching-Loss–Reduction Technique
- High-Efficiency Synchronous Mode Operation
- Fixed 1.4MHz Switching Frequency
- Can Synchronize to a 300kHz-to-3MHz External Clock
- Externally-Programmable Soft-Start
- OCP and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 Package

Pinning



Package Pin #	Name	Description
1	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch-mode regulator.
2	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP1498 operates from a +4.5V to +16V input rail. Requires a low-ESR, and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the PWM duty cycle ON time. The inductor current drives the SW pin negative during the OFF time. The low-side switch's ON-resistance and the internal body diode fix the negative voltage. Use wide PCB traces and multiple vias.
4	GND	System Ground. The regulated output voltage reference ground. Connect to GND with copper and vias.
5	BST	Bootstrap. Connect a capacitor between SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable. EN=high to enable the MP1498. Apply an external clock to change the switching frequency. For automatic start-up, connect EN pin to V_{IN} with 100KΩ resistor.
7	VCC	Internal 5V LDO Output. Powers the driver and control circuits. Decouple with a 0.1μF-0.22μF capacitor. Avoid capacitor values that exceed 0.22μF.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. The comparator lowers the oscillator frequency linearly with the FB voltage. It is recommended to place the resistor divider as close to FB pin as possible. Avoid placing vias on the FB traces.

Electrical Characteristics

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	µA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.8	1	mA
HS-Switch ON Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		100		mΩ
LS-Switch ON Resistance	LS_{RDS-ON}	V_{CC}=5V		40		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	µA
Current Limit [5]	I_{LIMIT}	Under 40% Duty Cycle	3.4			A
Oscillator Frequency	f_{SW}		1100	1400	1700	kHz
Fold-back Frequency	f_{FB}	V_{FB}= 0V		0.15		f_{SW}
Maximum Duty Cycle [6]	D_{MAX}	V_{FB}=700mV		89		%
Minimum ON Time [5]	t_{ON_MIN}			40		ns
Sync Frequency Range	f_{SYNC}		0.3		3	MHz
Feedback Voltage	V_{FB}	T_A=25°C	784	800	816	mV
		-40°C<T_A<85°C [7]	780	800	820	
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.1	1.25	1.4	V
EN Input Current	I_{EN}	V_{EN}=2V		2		µA
		V_{EN}=0		0		µA
EN Turn Off Delay	EN_{T_OFF}			5		µs
V_{IN} Under-Voltage Lockout Threshold-Rising	$INUV_{VTH}$		3.7	3.9	4.1	V
V_{IN} Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		3		%
Soft-Start Current	I_{SS}		10	14	18	µA
Thermal Shutdown [8]				150		°C
Thermal Hysteresis [8]				20		°C

C. TLV70033 (U107)

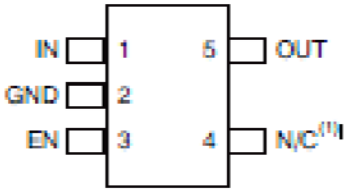
The TLV700xx series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Features

- Very Low Dropout:
  43 mV at I_{OUT} = 50 mA, V_{OUT} = 2.8 V
  85 mV at I_{OUT} = 100 mA, V_{OUT} = 2.8 V
  175 mV at I_{OUT} = 200 mA, V_{OUT} = 2.35 V
- 2% Accuracy
- Low I_Q: 31 µA
- Available in Fixed-Output Voltages from 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz

Pin Description and Package View

DCK PACKAGE
SC70-5
(TOP VIEW)



NAME	SON-6 DSE	SC70-5 DCK	TSOT23-5 DDC	DESCRIPTION
IN	1	1	1	Input pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	2	2	Ground pin
EN	6	3	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal.
NC	4, 5	4	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	3	5	5	Regulated output voltage pin. A small 1-µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

Electrical Characteristics

At V_{IN} = $V_{OUT(Typ)}$ + 0.3 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1.0 µF, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.0		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ +125°C	–2		+2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 200 mA		1	15	mV
V_{DO}	Dropout voltage[1]	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50 mA, V_{OUT} = 2.8 V		43		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100 mA, V_{OUT} = 2.8 V		85		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, V_{OUT} = 2.35 V		175	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	220		660	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		31	55	µA
		I_{OUT} = 200 mA, V_{IN} = V_{OUT} + 0.5 V		270		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2.0 V		400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V		1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Startup time[2]	C_{OUT} = 1.0 µF, I_{OUT} = 200 mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04	0.5	µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature		–40		+125	°C

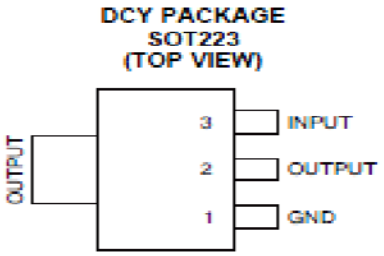
D. TLV1117LV15 (U111)

The TLV1117LV series of low-dropout (LDO) linear regulators is a low input voltage version of the popular 1117 voltage regulator. The TLV1117LV is an extremely low-power device that consumes 500 times lower quiescent current than traditional 1117 voltage regulators, making it suitable for applications that mandate very low standby current. The TLV1117LV family of LDOs is also stable with 0 mA of load current; there is no minimum load requirement, making it an ideal choice for applications where the regulator is required to power very small loads during standby in addition to large currents on the order of 1 A during normal operation. The TLV1117LV offers excellent line and load transient performance, resulting in very small magnitude undershoots and overshoots of output voltage when the load current requirement changes from less than 1 mA to more than 500 mA.

Features

- 1.5% Typical Accuracy
- Low IQ: 100 µA (max)
- 500 times lower than standard 1117 devices
- VIN: 2.0 V to 5.5 V
- Absolute maximum VIN = 6.0 V
- Stable with 0-mA Output Current
- Low Dropout: 455 mV at 1 A for VOUT = 3.3 V
- High PSRR: 65 dB at 1 kHz
- Minimum Ensured Current Limit: 1.1 A
- Stable with Cost-Effective Ceramic Capacitors:
- With 0-Ω ESR
- Thermal Shutdown and Over current Protection

Pin Description and Package View



TLV1117LV[1]		DESCRIPTION
NAME	TLV1117LVDCY	
IN	3	Input pin. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
OUT	2, Tab	Regulated output voltage pin. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	1	Ground pin

Electrical Characteristics

PARAMETER		TEST CONDITIONS			TLV1117LV Series MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.0		5.5	V
V_{OUT}	DC output accuracy	V_{OUT} > 2 V			–1.5		+1.5	%
		1.5 V ≤ V_{OUT} < 2 V			–2		+2	%
		1.2 V ≤ V_{OUT} < 1.5 V			–40		+40	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA				1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 1 A				1	35	mV
V_{DO}	Dropout voltage[1]	V_{IN} = 0.98 x $V_{OUT(NOM)}$	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		115		mV
				I_{OUT} = 500 mA		285		mV
				I_{OUT} = 800 mA		455		mV
				I_{OUT} = 1 A		570	800	mV
			V_{OUT} ≥ 3.3 V	I_{OUT} = 200 mA		90		mV
				I_{OUT} = 500 mA		230		mV
				I_{OUT} = 800 mA		365		mV
				I_{OUT} = 1 A		455	700	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			1.1			A
I_Q	Quiescent current	I_{OUT} = 0 mA				50	100	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA, f = 100 Hz				65		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 2.8 V, V_{OUT} = 1.8 V, I_{OUT} = 500 mA				60		μV_{RMS}
t_{STR}	Startup time[2]	C_{OUT} = 1.0 µF, I_{OUT} = 1 A				100		µs
UVLO	Undervoltage lockout	V_{IN} rising				1.95		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing				+165		°C
		Reset, temperature decreasing				+145		°C
T_J	Operating junction temperature				–40		+125	°C

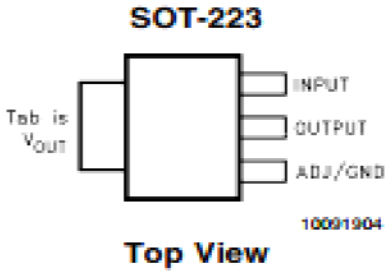
E. LM1117 (U102 & U105)

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed band gap reference to assure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I −40°C to 125°C

Pin Description and Package View



Top View

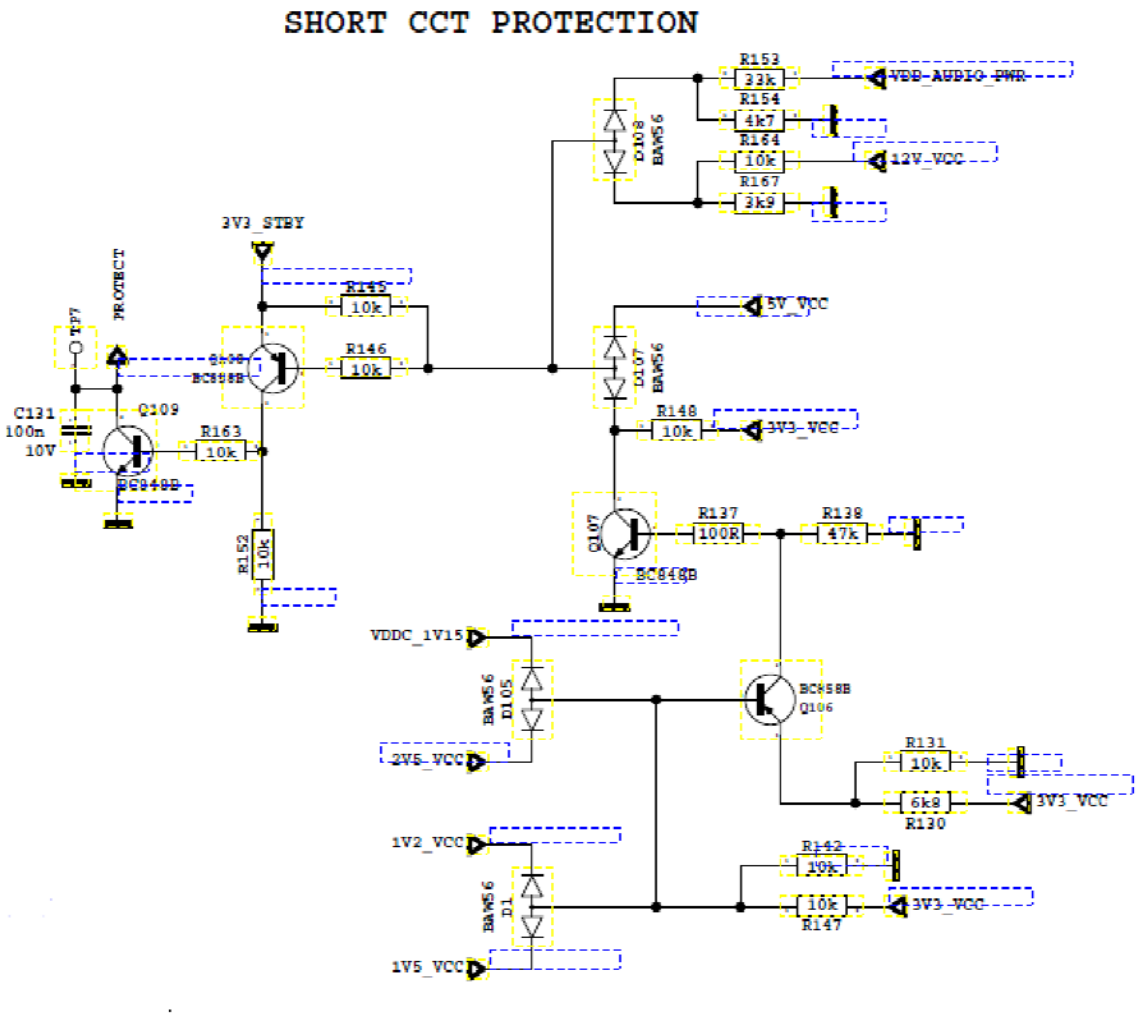
Electrical Characteristics

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{REF}	Reference Voltage	LM1117-ADJ I_{OUT} = 10mA, V_{IN}-V_{OUT} = 2V, T_J = 25°C 10mA ≤ I_{OUT} ≤ 800mA, 1.4V ≤ V_{IN}-V_{OUT} ≤ 10V	1.238 **1.225**	1.250 1.250	1.262 **1.270**	V V
V_{OUT}	Output Voltage	LM1117-1.8 I_{OUT} = 10mA, V_{IN} = 3.8V, T_J = 25°C 0 ≤ I_{OUT} ≤ 800mA, 3.2V ≤ V_{IN} ≤ 10V	1.782 **1.746**	1.800 1.800	1.818 **1.854**	V V
		LM1117-2.5 I_{OUT} = 10mA, V_{IN} = 4.5V, T_J = 25°C 0 ≤ I_{OUT} ≤ 800mA, 3.9V ≤ V_{IN} ≤ 10V	2.475 **2.450**	2.500 2.500	2.525 **2.550**	V V
		LM1117-2.85 I_{OUT} = 10mA, V_{IN} = 4.85V, T_J = 25°C 0 ≤ I_{OUT} ≤ 800mA, 4.25V ≤ V_{IN} ≤ 10V 0 ≤ I_{OUT} ≤ 500mA, V_{IN} = 4.10V	2.820 **2.790** **2.790**	2.850 2.850 2.850	2.880 **2.910** **2.910**	V V V
		LM1117-3.3 I_{OUT} = 10mA, V_{IN} = 5V T_J = 25°C 0 ≤ I_{OUT} ≤ 800mA, 4.75V≤ V_{IN} ≤ 10V	3.267 **3.235**	3.300 3.300	3.333 **3.365**	V V
		LM1117-5.0 I_{OUT} = 10mA, V_{IN} = 7V, T_J = 25°C 0 ≤ I_{OUT} ≤ 800mA, 6.5V ≤ V_{IN} ≤ 12V	4.950 **4.900**	5.000 5.000	5.050 **5.100**	V V
ΔV_{OUT}	Line Regulation (Note 6)	LM1117-ADJ I_{OUT} = 10mA, 1.5V ≤ V_{IN}-V_{OUT} ≤ 13.75V		0.035	**0.2**	%
		LM1117-1.8 I_{OUT} = 0mA, 3.2V ≤ V_{IN} ≤ 10V		1	**6**	mV
		LM1117-2.5 I_{OUT} = 0mA, 3.9V ≤ V_{IN} ≤ 10V		1	**6**	mV
		LM1117-2.85 I_{OUT} = 0mA, 4.25V ≤ V_{IN} ≤ 10V		1	**6**	mV
		LM1117-3.3 I_{OUT} = 0mA, 4.75V ≤ V_{IN} ≤ 15V		1	**6**	mV
		LM1117-5.0 I_{OUT} = 0mA, 6.5V ≤ V_{IN} ≤ 15V		1	**10**	mV

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
ΔV_{OUT}	Load Regulation (Note 6)	LM1117-ADJ V_{IN}-V_{OUT} = 3V, 10 ≤ I_{OUT} ≤ 800mA		0.2	**0.4**	%
		LM1117-1.8 V_{IN} = 3.2V, 0 ≤ I_{OUT} ≤ 800mA		1	**10**	mV
		LM1117-2.5 V_{IN} = 3.9V, 0 ≤ I_{OUT} ≤ 800mA		1	**10**	mV
		LM1117-2.85 V_{IN} = 4.25V, 0 ≤ I_{OUT} ≤ 800mA		1	**10**	mV
		LM1117-3.3 V_{IN} = 4.75V, 0 ≤ I_{OUT} ≤ 800mA		1	**10**	mV
		LM1117-5.0 V_{IN} = 6.5V, 0 ≤ I_{OUT} ≤ 800mA		1	**15**	mV
V_{IN}-V_{OUT}	Dropout Voltage (Note 7)	I_{OUT} = 100mA		1.10	**1.20**	V
		I_{OUT} = 500mA		1.15	**1.25**	V
		I_{OUT} = 800mA		1.20	**1.30**	V
I_{LIMIT}	Current Limit	V_{IN}-V_{OUT} = 5V, T_J = 25°C	800	1200	1500	mA
	Minimum Load Current (Note 8)	LM1117-ADJ V_{IN} = 15V		1.7	**5**	mA
	Quiescent Current	LM1117-1.8 V_{IN} ≤ 15V		5	**10**	mA
		LM1117-2.5 V_{IN} ≤ 15V		5	**10**	mA
		LM1117-2.85 V_{IN} ≤ 10V		5	**10**	mA
		LM1117-3.3 V_{IN} ≤ 15V		5	**10**	mA
		LM1117-5.0 V_{IN} ≤ 15V		5	**10**	mA
	Thermal Regulation	T_A = 25°C, 30ms Pulse		0.01	0.1	%/W
	Ripple Regulation	f_{RIPPLE} =120Hz, V_{IN}-V_{OUT} = 3V V_{RIPPLE} = $1V_{PP}$	**60**	75		dB
	Adjust Pin Current			60	**120**	µA
	Adjust Pin Current Change	10 ≤ I_{OUT} ≤ 800mA, 1.4V ≤ V_{IN}-V_{OUT} ≤ 10V		0.2	**5**	µA
	Temperature Stability			0.5		%
	Long Term Stability	T_A = 125°C, 1000Hrs		0.3		%
	RMS Output Noise	(% of V_{OUT}), 10Hz ≤ f ≤10kHz		0.003		%
	Thermal Resistance Junction-to-Case	3-Lead SOT-223		15.0		°C/W
		3-Lead TO-220		3.0		°C/W
		3-Lead TO-252		10		°C/W
	Thermal Resistance Junction-to-Ambient (No air flow)	3-Lead SOT-223 (No heat sink)		136		°C/W
		3-Lead TO-220 (No heat sink)		79		°C/W
		3-Lead TO-252 (Note 9) (No heat sink)		92		°C/W

8. SHORT CCT PROTECTION CIRCUIT

Short circuit protection is necessary for protecting chassis and main IC against damages when any Vcc supply shorts to ground. Protect pin should be logic high while normal operation. When there is a short circuit protect pin should be logic low. After any short detection, SW forces the system to go into standby mode and to indicate short circuit detection LEDs on LED card blinked in a determined sequence.



9. MICROCONTROLLER – Novatek

A. NT72567 (MAIN IC) (U112)

The NT72567 is an integrated digital TV system-on-chip which compliants with variety ATV as NTSC, PAL and SECAM, and DTV standards as ISDB-T, DVB-T/-C, ITU-T J.83B, integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing.

The integrated video ADC and video decoder support PC VGA port, YPbPr, SCART, CVBS and S-Video Input. Regarding the tuner input, The digital VIF performs the universal analog TV demodulation (NTSC, PAL, and SECAM), including IF processing, AGC, video demodulation, and second sound IF generation (SSIF). The video decoder supports universal TV video format. The integrated audio ADC supports stereo audio input corresponding to video input sources. The integrated TV sound decoder supports universal TV sound format.

The advanced picture quality and color engine create more vivid image impression than ever. The HDMI receiver v1.4a supports deep color, CEC features and 3D formats. The USB high speed host supports updating firmware code, multi-media playback from the external USB flash devices.

The standby controller can operate solely from the main system, powered by the standby power source from power module, consumes as low current as possible. It meets the requirement of Green appliance.

General Features:

- Internal High-Speed ADC
    - Integrated triple high speed ADCs/ PLL to support both YPbPr and RGB format signal
    - 10-bits data resolution
    - Maximum conversion up to 165 MSPS
    - Support 0.7 ~ 1.0 Volts analog RGB/YUV input
    - Guaranteed No Missing Code
    - 3:1 analog input MUX
    - Ultra Low PLL Jitter @210MHz
    - Supports both non-interlaced and interlaced input signals
    - Digital PLL with 64 steps of phase adjustment for each channel

- Analog Video Decoder
    - Clamp and AGC (Automatic Gain Control) circuit to support 0.5 to 1.6V analog input signal
    - Support multi-standards, macro-vision detection and related status report
    - Embedded Teletext Level 2.5 / Close Caption and other VBI Decoder
    - 2D and 3D adaptive Comb Filter for better Y/C Separation
    - Maximum two SCART input
    - Support VPS signal decode for EU channel sorting purpose

- Digital VIF Support general IF, 38.9 MHz, 45.75 MHz, and 33.1 MHz (can tuner with a digital-SAW filter)
    - Support Low IF, 5 ~ 8 MHz (silicon tuner)
    - Support dual AGC (RF and IF) with programmable PWM
    - Flexible channel bandwidth (6 MHz, 7 MHz, and 8 MHz)
    - Digital video/audio splitting

- SIF Decoder
    - NICAM-BG/DK/I/L, A2-BG/DK/I, BTSC, EIA-J, A2-M, AM SECAM-L
    - Automatic standard and mode detection
    - Automatic carrier mute and automatic NICAM fall back
    - 32KHz audio output

- ISDB-T(SE2 confirmed)
    - ISDB-T standard ARIB STD-B31
    - SBTVD standard ABNT NBR 15601
    - Receiver specifications ARIB STD-B21 & ABNT NBR 15604 fulfilled
    - Channel bandwidth 6, 7 & 8 MHz supported
    - Zero IF & nonzero IF with configurable mixing frequency
    - Single IF AGC or dual RF/IF AGC controls with Delta modulation
    - Partial (1-segment) & full (13-segment) reception supported
    - Non-hierarchical (single-layer) & hierarchical (layers A/B/C) reception supported

- DVB-T Demodulator
    - Compliant with ETSI EN 300 744, NorDig Unified V.2, and D-book V.6
    - Automatic transmission parameter detection
        - 2K/8K modes
        - Guard intervals of 1/4, 1/8, 1/16, 1/32
        - All hierarchical and non-hierarchical constellations
        - Code rates of 1/2, 2/3, 3/4, 5/6, 7/8
    - Single IF AGC or dual RF/IF AGC controls
    - Direct IF (36.167MHz or 43.75MHz) or low IF (4.57MHz) support
    - Impulsive noise reduction
    - Adjacent channel interference (ACI) filter and Co-channel interference (CCI) suppression
    - RF signal strength monitoring
    - Support power saving mode

- DVB-C Demodulator
    - Compliant with ETSI EN 300 429 DVB-C and ITU-T J.83 annex A/C Standards
    - Support Direct IF/Low IF Sampling
    - Programmable Digital Mixer
    - Single IF AGC or dual RF/IF AGC controls

- Variable Symbol Rate 1 MBaud ~ 7.2 MBaud Support
- Matched Filters (Roll-off factor= 0.15, 0.13)
- Superior Carrier Recovery, Acquisition range up to 5%(Symbol Rate)
- Robust Dual Adaptive Blind Equalizer (short echo/long echo)
- High monitoring capabilities
  - C/N ratio (SNR)
  - Signal Power
  - RS uncorrectable error Number

- Digital Video Decoder
  - Built-in multi-standard video codec
  - Support pixel format YUV420 only for all video codec except JPEG
  - H.264 Constrained Baseline/Main/High Profiles @ 1080p30 (Level 4.0 and Level 4.1 under limited bit-rate).
  - MVC Stereo High Profile @ 1080p48 and 720p120
  - VP8 All Profiles @ 1080p30.
  - AVS (Optional) Jizhun Profile @ 1080p30 (Level 6.0).
  - VC-1(Optional) Simple/Main/Advanced Profiles @ 1080p30 (Level 3.0).
  - Real Video (Optional) 8/9/10 @ 1080p30.
  - MPEG-4 Simple/Advanced Simple Profiles @ 1080p30.
  - H.263 Profile 0 @ 1080p30.
  - DivX 3/4/5/6 @ 1080p30(Optional).
  - Support GMC with 1 warp point.
  - Sorenson Spark @ 1080p30.
  - MPEG-2 Main Profile @ 1080p30.
  - MPEG-1 @ 1080p30.
  - JPEG baseline sequential mode.
    - Support pixel formats in YUV420, YUV422 and YUV444.
    - Support Motion JPEG @ 1080p30.

- Condition Access
  - Support Common Interface
  - Support Common Interface Plus
  - Built-in Cryptograph Engine for conditional access and CI Plus
  - Meet Common Interface Plus's Robust and Compliance rule

- Copy Protection Engine
    - Support Cryptograph Key Protection
    - Support Demux Key Protection
    - Support HDCP Key Protection

- External DRAM Interface 16 bit DDR3-SDRAM bus
    - 16bit DDR3-SDRAM bus
    - External DRAM Clock up to 533/666/800MHz
    - Spread Spectrum PLL for EMI reduction
    - Up to 4 Gb of DDR3-SDRAM density
    - Embedded 1Gb/2Gb DDR3-SDRAM(MCM or internal DDR)

- De-Interlacing
    - Support progressive scan 24Hz to 85Hz Frame Rate Conversion
    - 5th generation High performance Motion- Adaptive De-interlacing
    - 5th generation Diagonal Edge Enhancement for smoothing edge outline
    - Automatic Video Source Detection
    - Support Inverse 3:2/2:2 pull down and multiple cadence for film stream
    - Scene Change Detection
    - Built-in Anti-Cross color to remove abnormal color performance
    - Built-in Color Performance stabilizer for SECAM video format
    - Built-in Region Classifier engine to get flicker free image quality

- Visual Effect Processor
    - Built-in Advanced Super Resolution
    - 5th generation Advanced Scaling Up Engine
    - Support Nonlinear Scaling
    - 5th generation LTI/CTI function
    - Support 5th Color Engine
    - Global Brightness, Contrast, Hue Saturation and Intensity Adjustment
    - Built-in I-Gamma and Black Stretch for Automatic Contrast Adjustment
    - Support sRGB and xvYCC Adjustment Standard
    - De-blocking, De-Mosquito, Temporal and Spatial Noise Filter
    - Adaptively determine 3D noise filter for different noise level

- Linear Gamut Remapping
- SD2HD detection and Processing
- DP Meter for Dynamic backlight Control

- Display Processor
  - Embedded dual 10 bit LVDS transmitter
  - Supports single pixel / dual pixel output
  - Dithering function supports 30-bit quality for 24 bit or 18-bit panel
  - Optional Frame Sync or Free Run display synchronization modes
  - Display Resolution up to 1920x1200@60Hz and 1920x540@120Hz HDTV format
  - Built-in Gamma Correction for different type display device
  - Supports Pivot (H flipping display)
  - V flipping is in LBM
  - Support H/V sync out

- 2D-Graphic Engine / OSD
  - Bitmap Operation
    - ARGB/RGBA format
    - Copy/Color expansion
    - Logic Operation
    - Copy with alpha blending (only 16/32 bit color mode)
    - Source and destination area could be overlapped
    - Color key for the transparence effect
    - 12 Raster Operation (ROP) rules
  - Fill Rectangle
    - Color fill
    - Gradient fill
  - Scaling
    - Bicubic Algorithm
  - 8/16/32-bit OSD Architecture
  - 3 OSD Layers, each with 2 exclusive regions
  - 5 levels of transparency with pixel or frame based operation (background, video, Plane3, Plane2, Plane1)
  - Programmable width & height to meet LCD/TV's resolution exactly
  - H Bicubic scaling up and V Bilinear scaling

- Audio Interface
    - Built-in 5:1 audio ADC input mux (MAX. sampling rate 48KHz)
    - Built-in 2 audio DAC output (MAX. sampling rate 48KHz)
    - Built-in 3 I2S Output format for Power-Stage Amplifier
    - S/PDIF output supported

- Audio Processor
    - Dedicated DSP to decode compressed audio
    - 16KB instruction, 48KB data cache
    - Support ADPCM, MP3 decoder
    - Support AC3(Optional) / HE-AAC(Optional) audio format
    - Support Dolby2 Digital (Optional)/ WMA(Optional) audio format
    - DTS3(Optional)/ DTS-LBR3(Optional)
    - Automatic volume control
    - Virtual surround

- High performance 24Kec 32-bit CPU
    - Built-in Memory Management Unit
    - 16KB instruction and 16KB data cache
    - 128K L2 Cache

- Stand-by Controller
    - Support VGA / IR / Keypad / CEC/DDCCI wake-up
    - Built-in Turbo 8051 for stand-by application usage
    - Built-in Low Voltage Reset for brown out
    - Built-in EDID for saving system BOM cost
    - System power control

- TV encoder with built-in video DAC
    - Built-in 10-bit DAC for CVBS Analog Video output.
    - Support HD resolution input with high quality scaling down engine
    - Support TTX/ CC/ WSS/ VPS/ CGMS-A/Macrovision insertion

- Ethernet MAC
  - Built-in 10/100 Ethernet MAC
  - Compatible with IEEE 802.3
  - Support RMII interface with front-end Ethernet PHY

- USB host/device controller with built in transceiver
  - 2 USB host ports
  - Compliant with USB Specification Revision 2.0
  - Support high-speed, full-speed and low-speed devices
  - Integrated USB 2.0 transceiver

- HDMI receiver
  - Three HDMI Input ports(Port A is HDMI &MHL combo port)
  - HDMI 1.4a Compliant
  - Integrated HDCP 1.1 cipher engine for Content Protection
  - Support High-Level CEC Command for Easy Link between CE equipments.
  - Support Deep Color for more pixel depth information
  - Support xvYCC for wide color gamut application
  - 3D support
  - Support Audio format including
    - 2~8 -channel 32-192KHz
  - Support ARC (Audio Return Channel)

- MHL receiver
  - CBUS
    - DDC packet
    - MSC(MHL Sideband Channel) packet
    - Vendor-specific packet
  - VBUS

- Memory controller
  - NAND type flash
    - RS Support
    - RS Read Free Run
    - 4Bytes/512Byte ECC

        - Timing Fine Tune
    - eMMC 4.41(Optional) type flash
    - SPI NOR type flash

- 3D support
    - 2D-to-3D real time conversion
    - Support mandatory HDMI 1.4a 3D video format and timing
        - 3DFP
        - 3D SBS
        - 3DTB
    - Support 100/120Hz shutter glasses half FHD 3D TV panel
    - Line interleave for directly drive 60Hz PR 3D LCD
    - Intermediate formats output support external 3D processor
    - Support separate and programmable L/R sync pin
    - Support Shutter glasses control signals
        - L/R sync signal phase, polarity, duration programmable
        - Samsung IR protocol support

- LZ77 Decompression engine
    - 250 MByte/sec
    - MAX search window buffer 512 byte
    - MAX search length 18

- LED backlight
    - PWM x 8
    - PWM delay and duty is adjustable independently
    - PWM delay is phase-locked to VS
    - support PWM frequency = 1 x VS , 2 x VS frequency
    - support I2C/SPI LED-driver interface

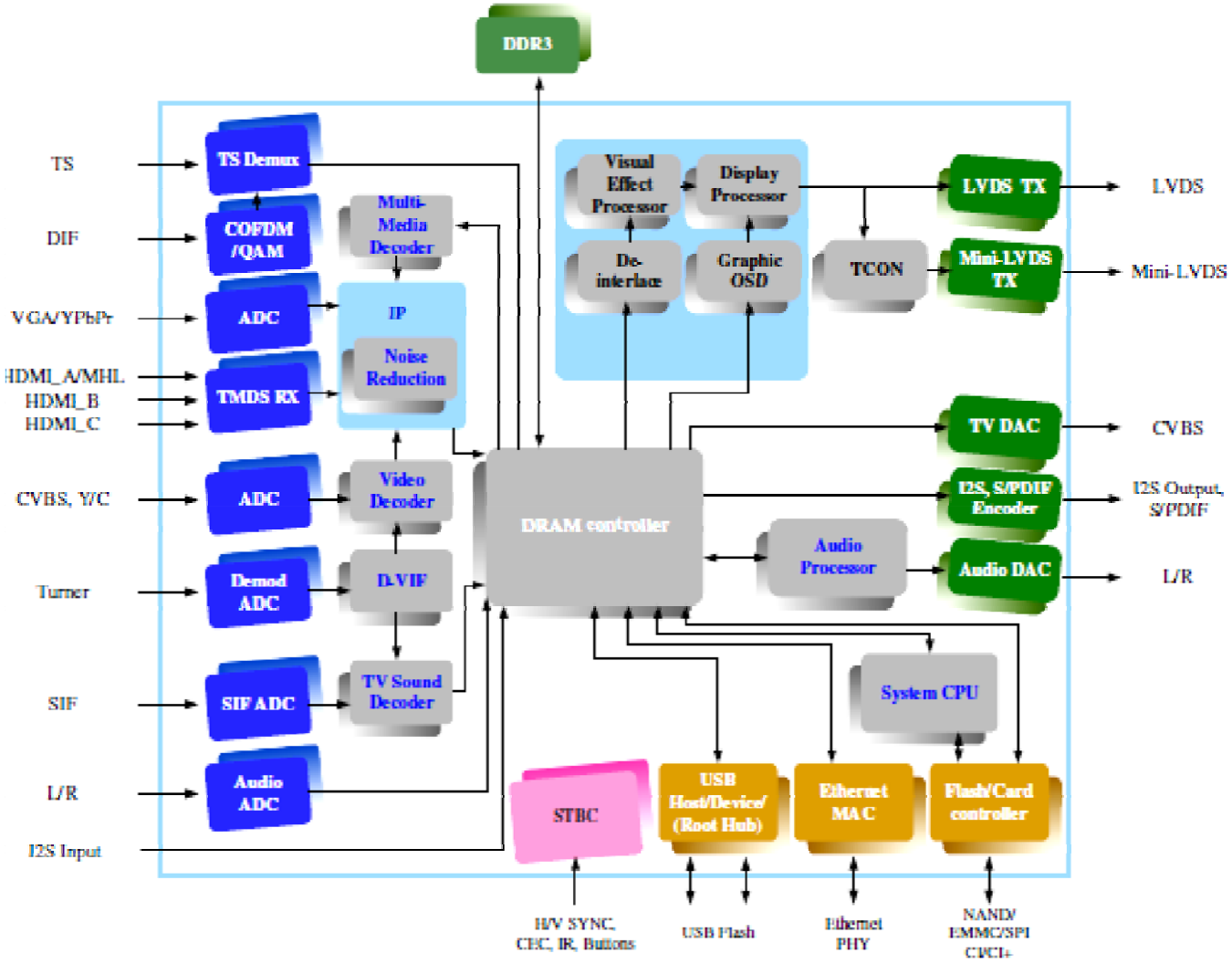
- TCON
    - Support fail-safe mode function.
    - Support Built-in 2-port 6-pair mini-LVDS output.
    - Support Resolution: FHD(1920X1080) & HD(1366X768)
    - Support over-driving function for improving LCD response time.

- Support data compression function for reducing frame data storage.
- Support gamma function that provides 12-bit full range programming.
- Support Built-in spread spectrum clock generator to lower the EMI issue.
- Support CABC(Content Adaptive Brightness Control) function
- Support mini-LVDS output Data-Skew control.
- Support 1 line, 2 line, 1+2 line, and frame inversion mode.
- support 8bit and 6 bit
- support 3D frame-sequential output and 2D output
- support 50Hz, 60Hz, 100Hz, 120Hz

- Miscellaneous
  - Built-in UART controller
  - LFBGA 21x21 - 576 balls

- Electrical and Physical Characteristics
  - Single 12 MHz clock input crystal
  - 1.15/1.5/2.5/3.3V power supply
  - Power standby mode
  - LFBGA-576

Novatek NT72567 Block Diagram



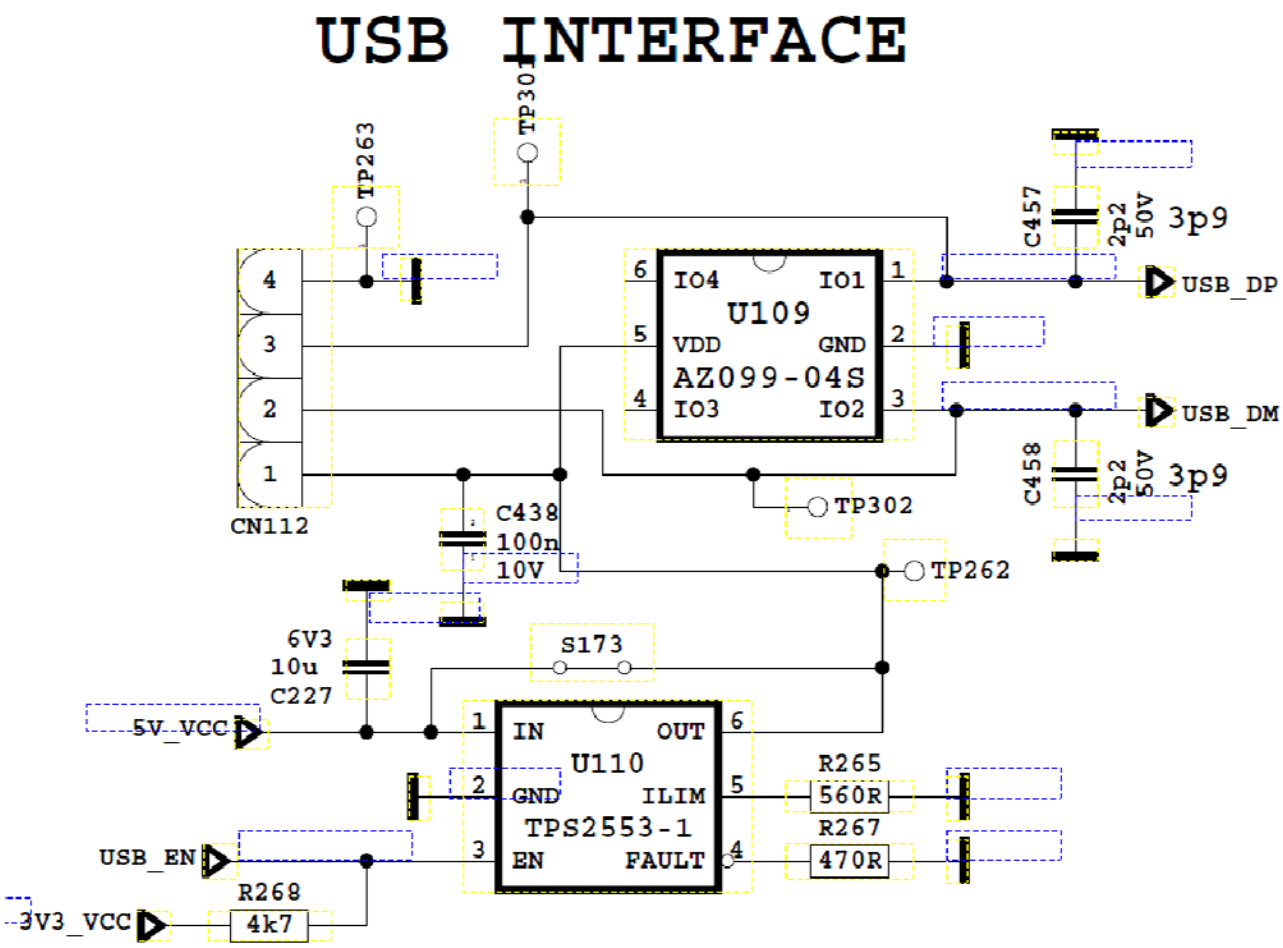
10. USB INTERFACE

Main Concept IC has integrated 2 USB 2.0 interface. One of them is used for Ethernet function, the other one is used for USB connectivity for last user. Last user can play video, picture and audio files. Also digital channels can be record to external storage device by this interface. All SW files can be updated with interface.

USB circuit has 3 main parts

- Integrated USB 2.0 Host interface of NT72567 (U112)
- Protection IC (U109) (optional*)
- Over Current Protection IC (U110) (optional*)

* The max current that can be supplied for USB loads does not cause a danger for main IC. So, these ICs are used as optional.



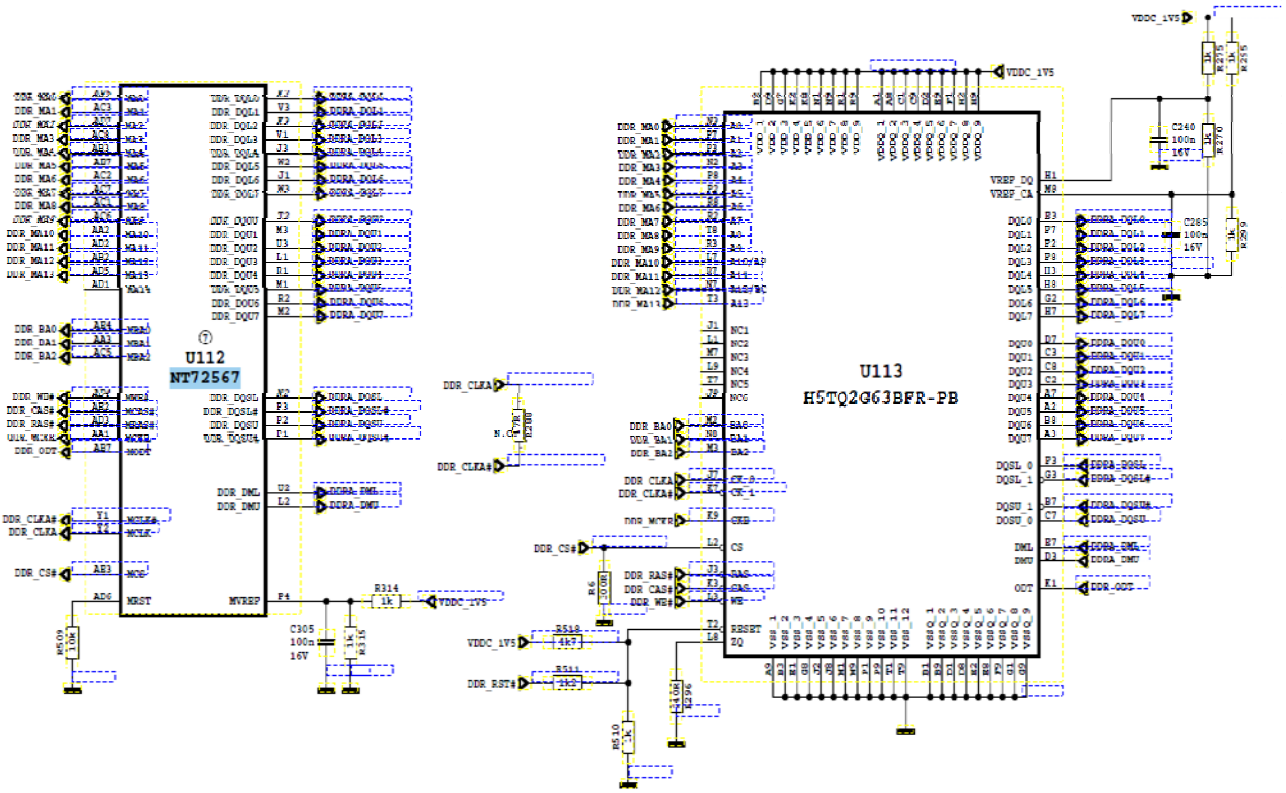
11. DDR3 SDRAM K4B1G1646G 1GB G-DIE (U113)

The 1 GB DDR3 SDRAM G-die is organized as a 8Mbit x 16 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2133Mb/sec/pin (DDR3-2133) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset . All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V VDDQ. The 1 GB DDR3 G-die device is available in 96ball FBGA(x16).

Features

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin, 933MHz f_{CK} for 1866Mb/sec/pin, 1066MHz f_{CK} for 2133Mb/sec/pin

- 8 Banks
- Programmable CAS Latency (posted CAS): 5,6,7,8,9,10,11,13,14
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600), 9(DDR3-1866) and 10(DDR3-2133)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with t_{CCD} = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal (self) calibration: Internal self calibration through ZQ pin
- (RZQ: 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
- Support Industrial Temp (-40 ~ 85°C)
- Asynchronous Reset
- Package: 96 balls FBGA - x16
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free



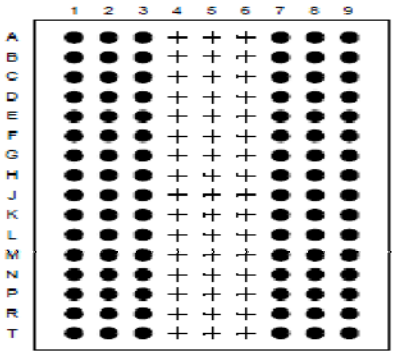
Pinning

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{DQSU}$	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	$\overline{DQSL}$				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	J
K	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	K
L	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	L
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	$\overline{RESET}$	A13				NC	A8	V_{SS}	T

Ball Locations (x16)

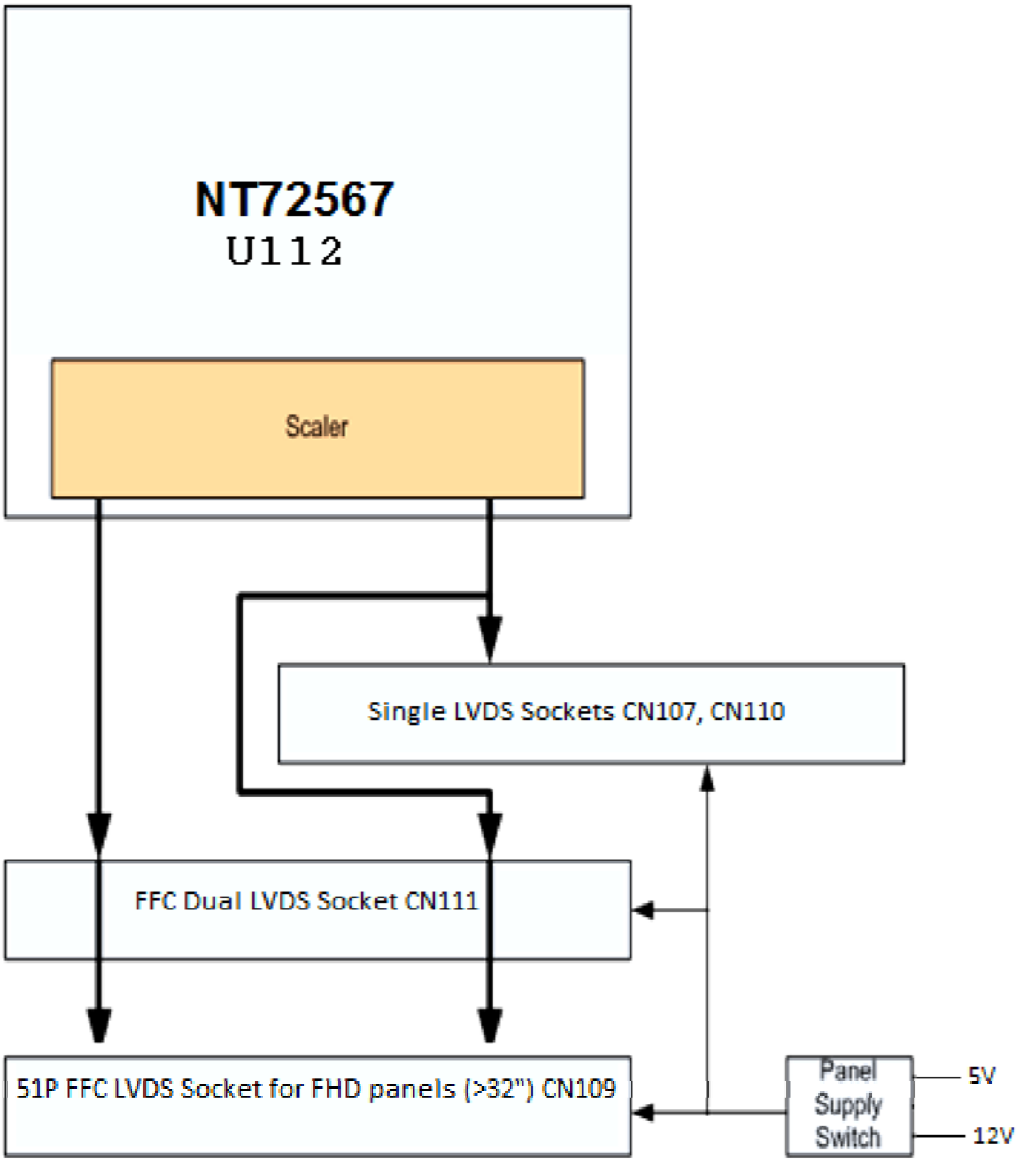
● Populated ball
+ Ball not populated

Top view
(See the balls through the package)



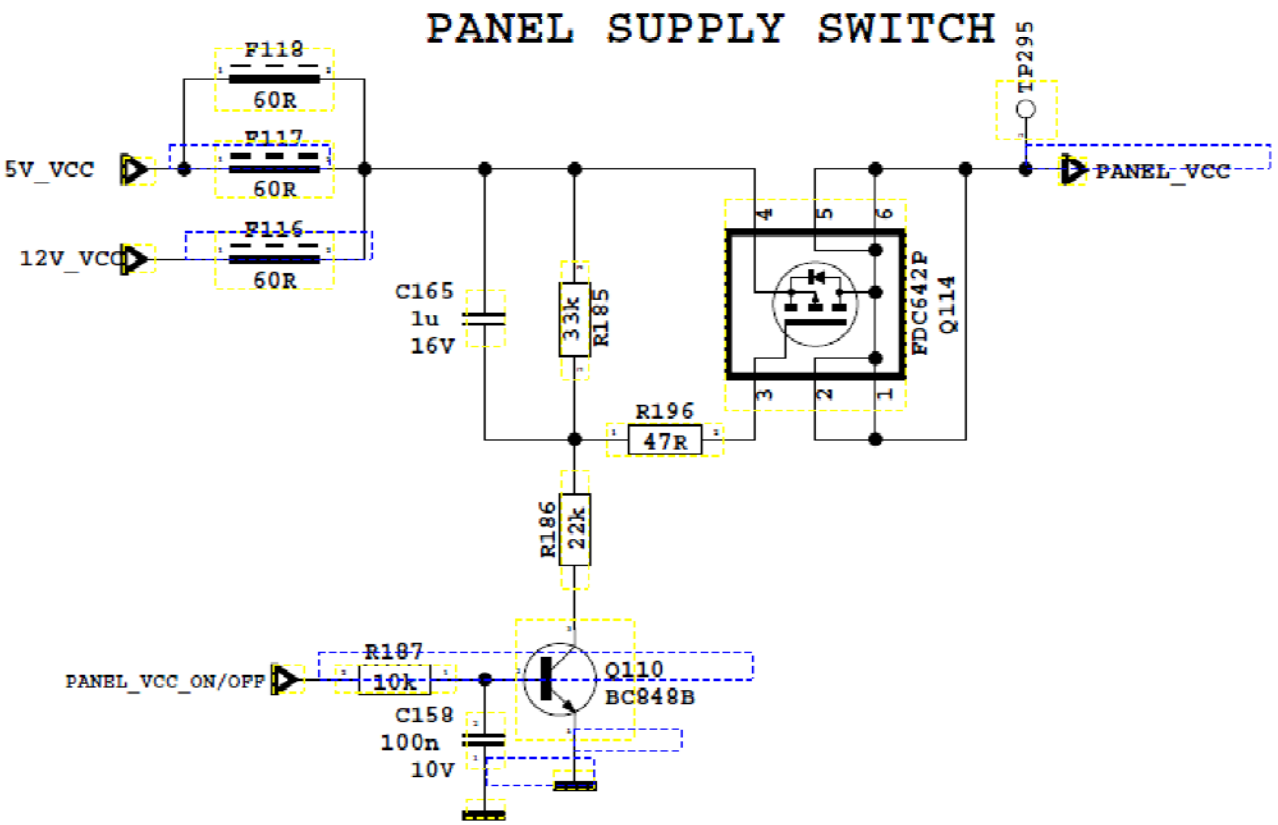
12. SCALER AND LVDS SOCKETS

LVDS Sockets Block Diagram

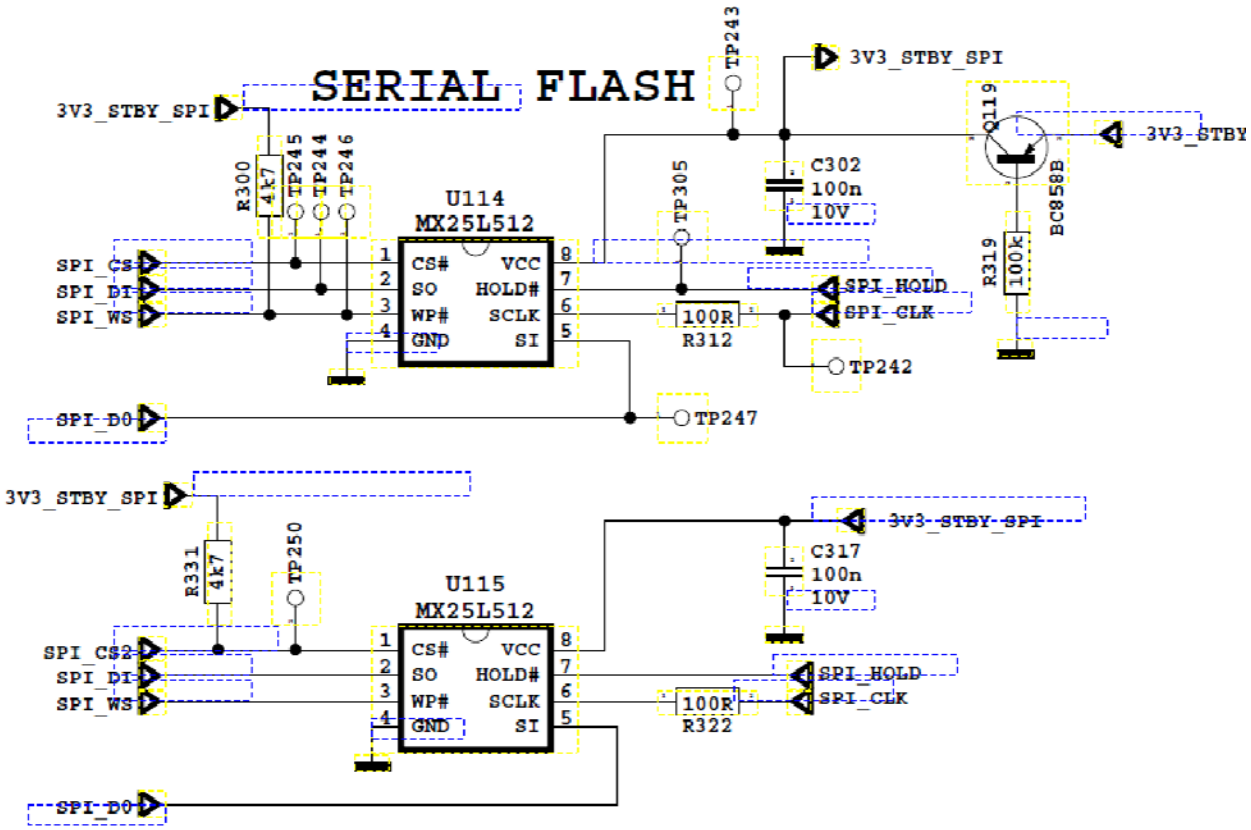


13. PANEL SUPPLY SWITCH CIRCUIT

This switch is used to open and close panel supply of TCON. It is controlled by port of main µcontroller. Also, with this circuit, the panel power sequences could be adjusted correctly. 2 panel supply options are connected to the circuit. All of them are optional according to panels.



14. SPI FLASH MEMORY



A. 3V 64M-BIT SERIAL FLASH MEMORY WITH DUAL/QUAD SPI & QPI (U114)

General Description

The W25Q64FV (64M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q64FV array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q64FV has 2,048 erasable sectors and 128 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

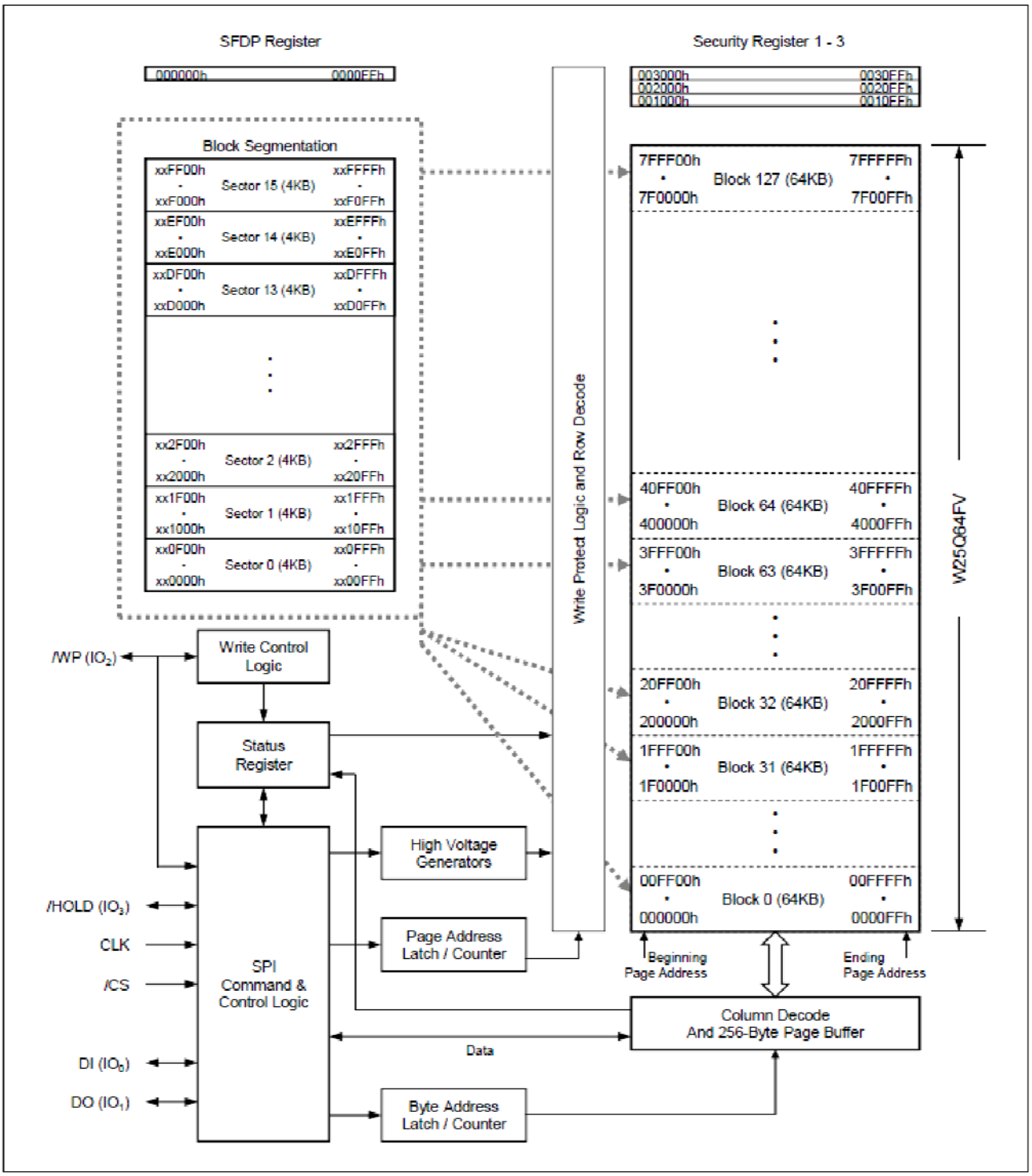
The W25Q64FV support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification, a 64-bit Unique Serial Number and four 256-bytes Security Registers.

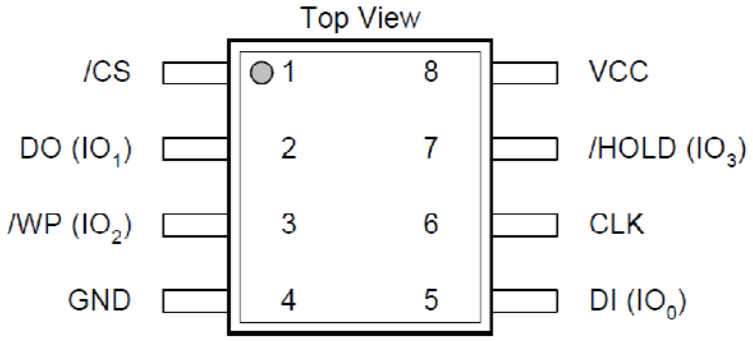
Features

- **Family of SpiFlash Memories**
  - W25Q64FV: 64M-bit / 8M-byte (8,388,608)
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- **Highest Performance Serial Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-bytes)
  - Uniform Block Erase (32K and 64K-bytes)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB complement array protection
  - Power Supply Lock-Down and OTP protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC/VSOP 208-mil
  - 8-pad WSON 6x5-mm/8x6-mm
  - 16-pin SOIC 300-mil
  - 8-pin PDIP 300-mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for KGD and other options

Block Diagram



Pinning



PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

B. 3V 32M-BIT SERIAL FLASH MEMORY WITH DUAL/QUAD SPI & QPI (U115)

General Description

The W25Q32FV (32M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q32FV array is organized into 16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q32FV has 1,024 erasable sectors and 64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

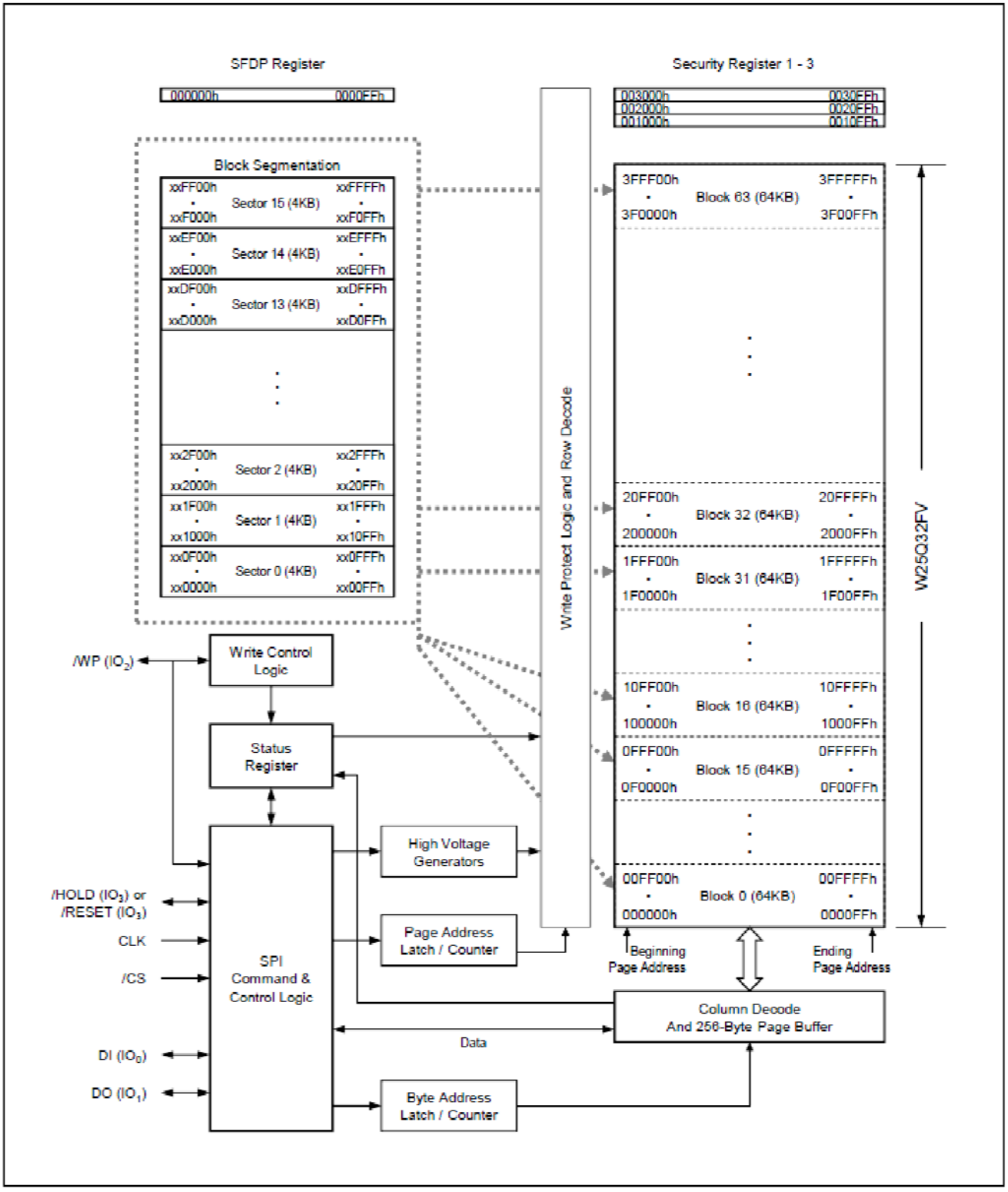
The W25Q32FV support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

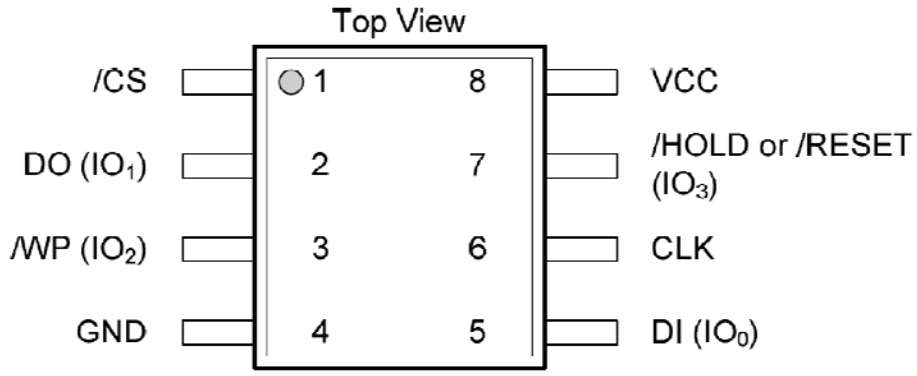
Features

- **New Family of SpiFlash Memories**
  - W25Q32FV: 32M-bit / 4M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software & Hardware Reset
- **Highest Performance Serial Flash**
  - 104MHz Single, Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil / VSOP 208-mil
  - 8-pad WSON 6x5-mm / 8x6-mm
  - 16-pin SOIC 300-mil (additional /RESET pin)
  - 8-pin PDIP 300-mil
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGD and other options

Block Diagram



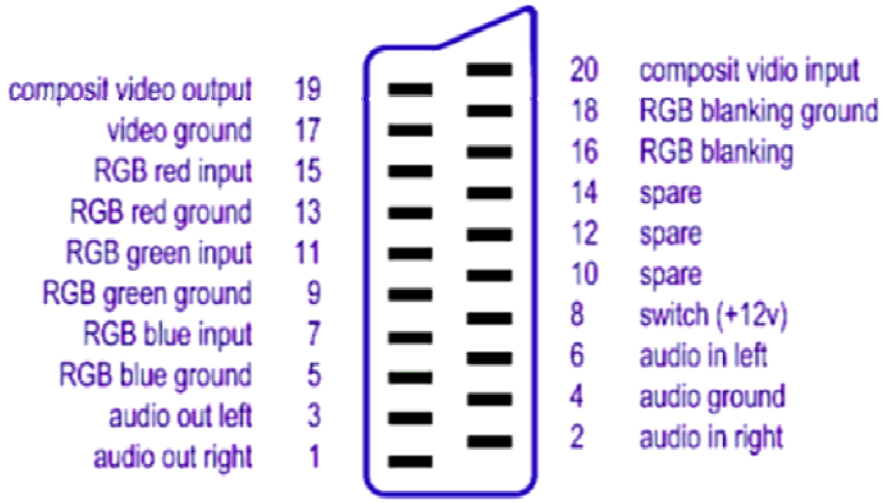
Pinning



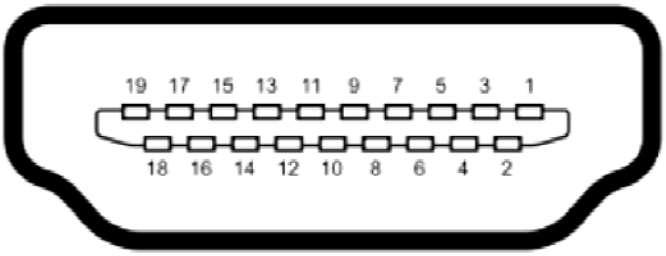
PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

15. CONNECTORS

A. SCART (SC100)

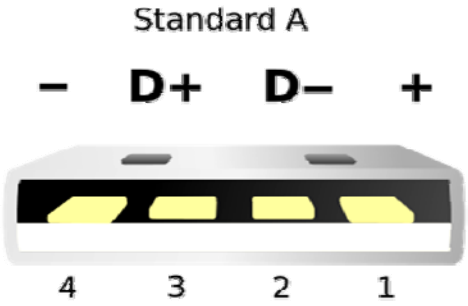


B. HDMI (CN115, CN116)



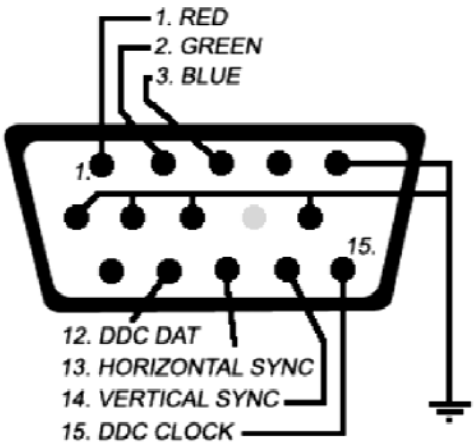
Pin Number	Signal Name	Pin Number	Signal Name
1	TMDS Data 2+	20	SHELL
2	TMDS Data 2 Shield	19	Hot Plug Detect
3	TMDS Data 2-	18	+5V Power
4	TMDS Data 1+	17	Ground
5	TMDS Data 1 Shield	16	DDC Data
6	TMDS Data 1-	15	DDC Clock
7	TMDS Data 0+	14	No Connect
8	TMDS Data 0 Shield	13	CEC
9	TMDS Data 0-	12	TMDS Clock-
10	TMDS Clock+	11	TMDS Clock Shield

C. USB (CN112)

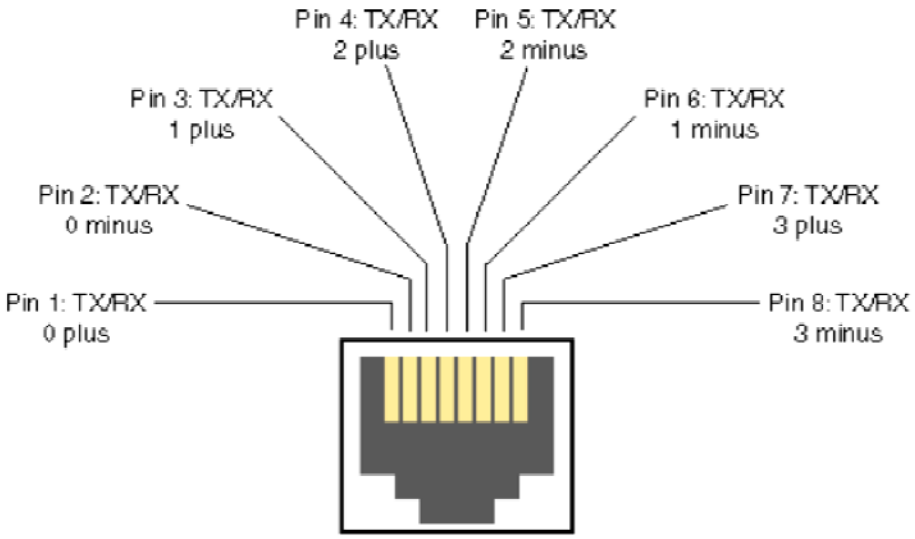


Pin	Name	Cable color	Description
1	VBUS	Red	5 V
2	D-	White (gold*)	Data −
3	D+	Green	Data+
4	GND	Black (blue*)	Ground

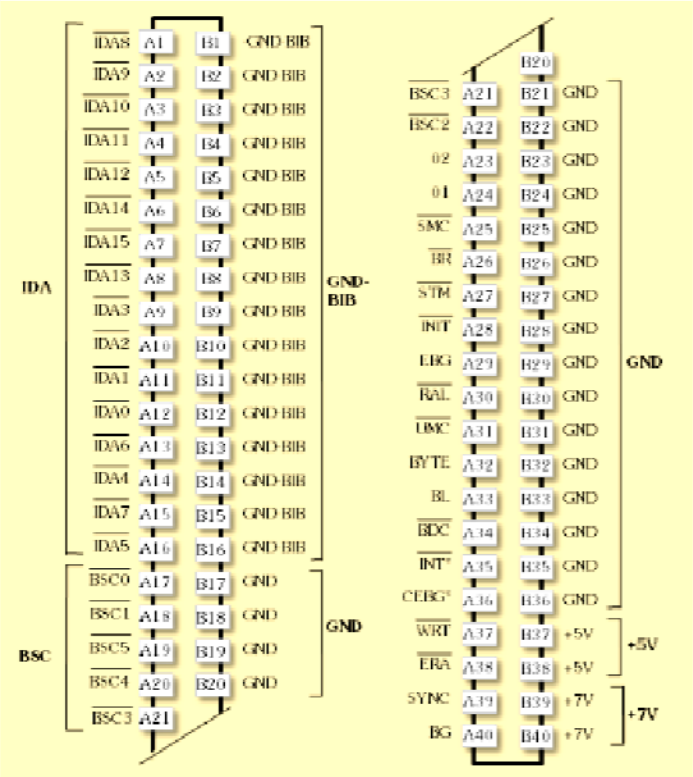
D. *VGA (CN117)*



E. *ETHERNET (CN114)*



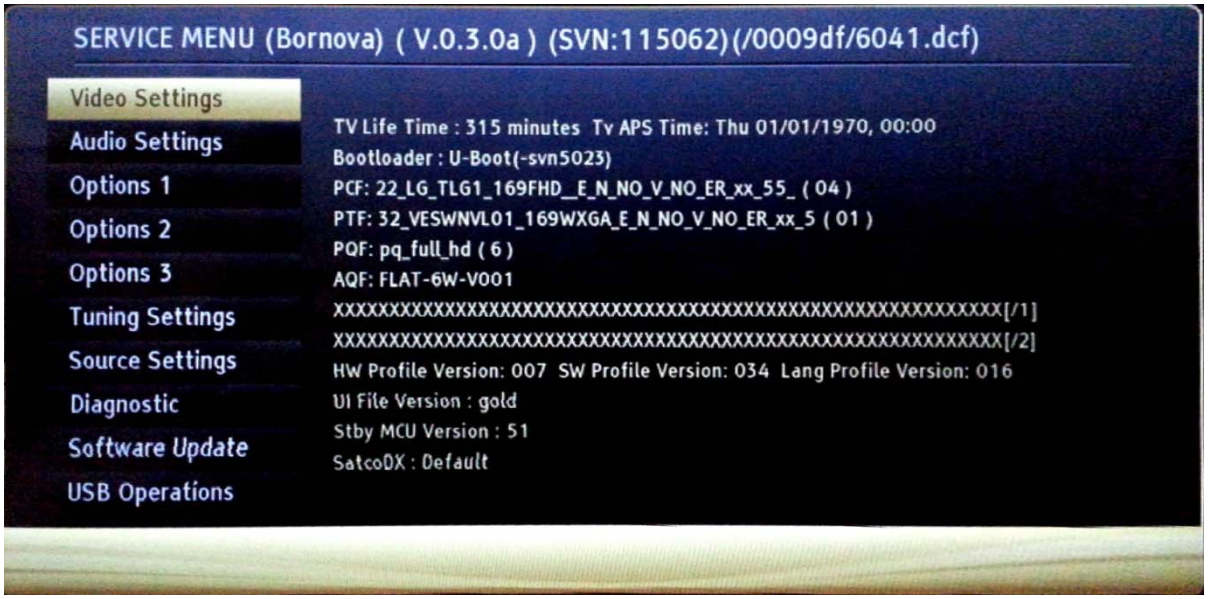
F. *COMMON INTERFACE (CI) (CN106)*



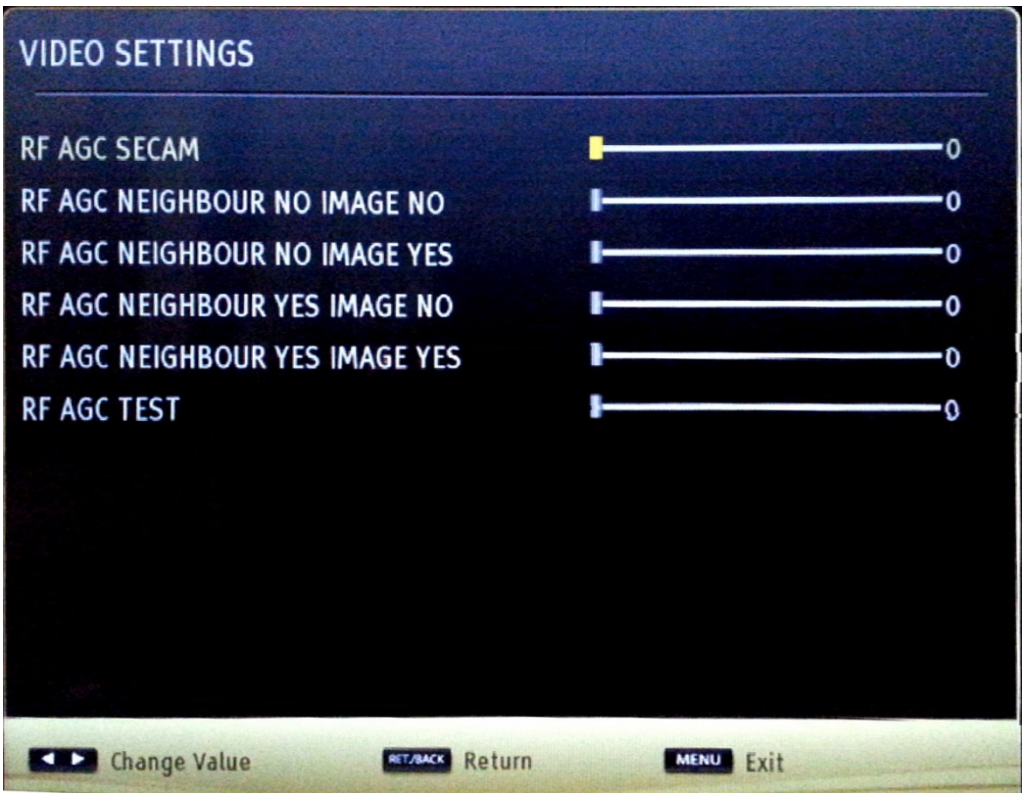
16. SERVICE MENU SETTINGS

In order to reach the service menu, first press “MENU” button, then press “4725” from the remote controller keypad.

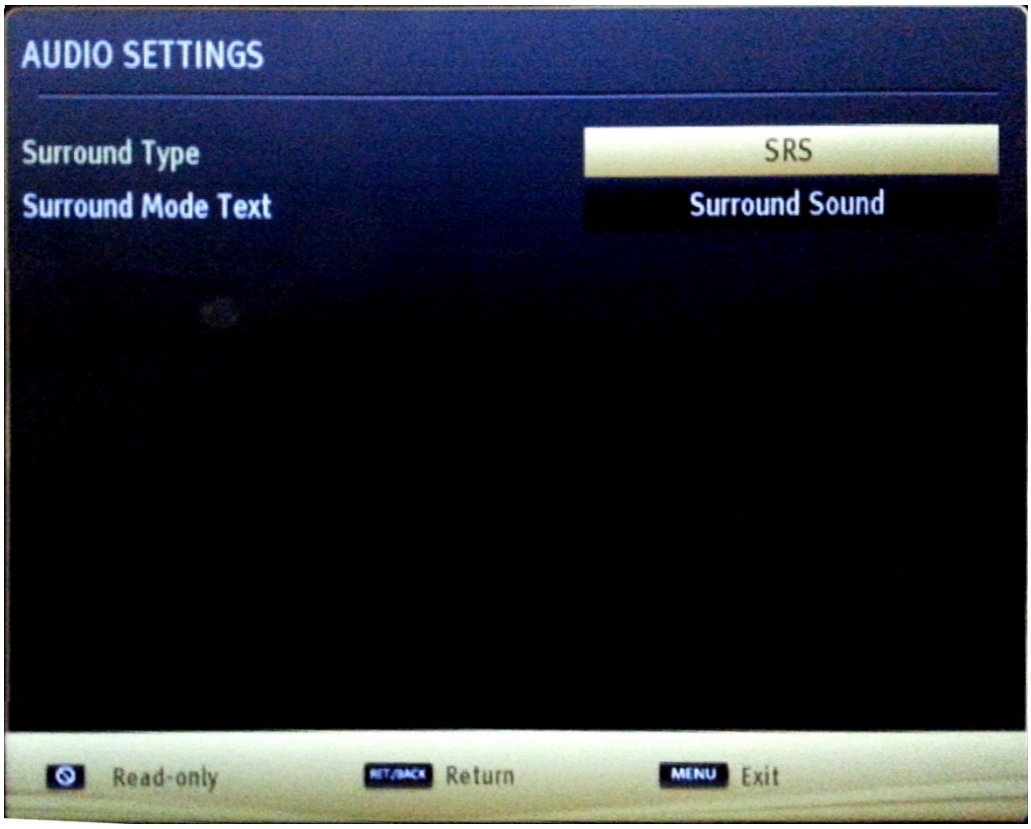
Following setting options be seen as below.



A. *VIDEO SETTINGS*

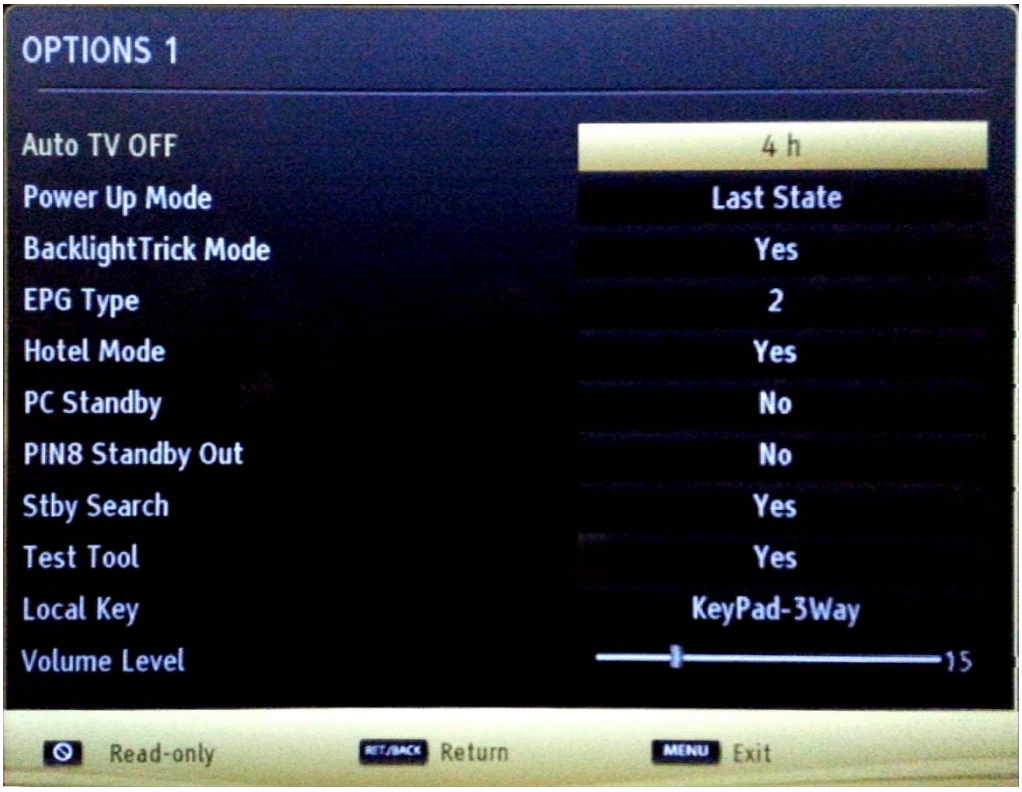


B. *AUDIO SETTINGS*

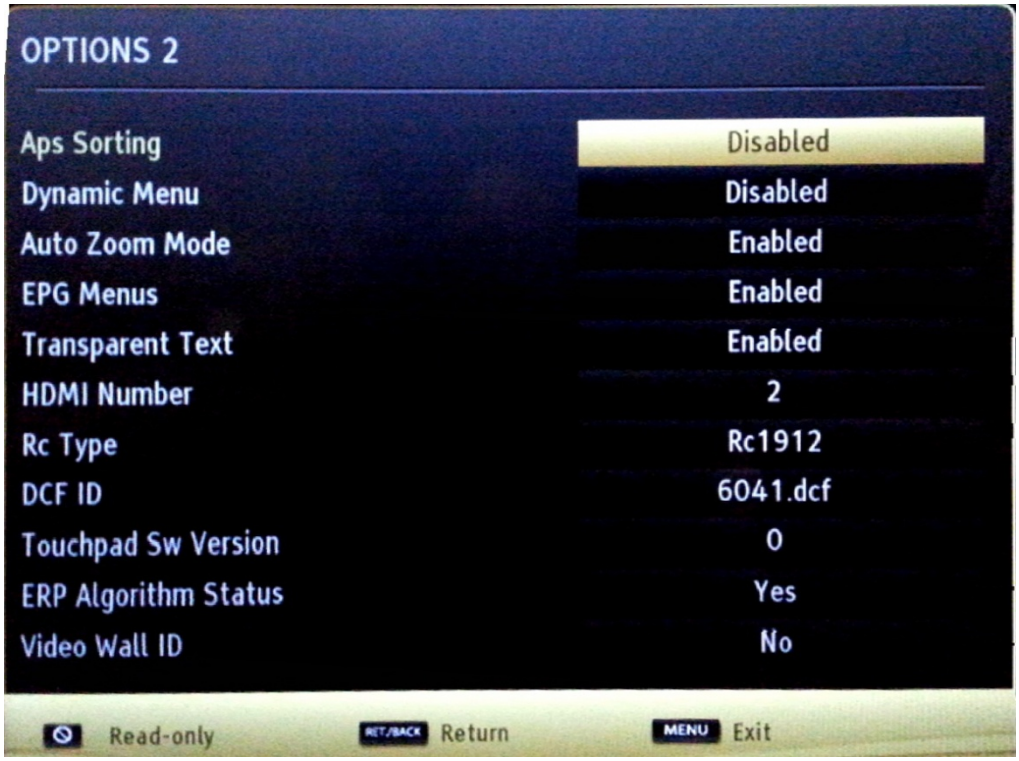


C. OPTIONS SETTINGS

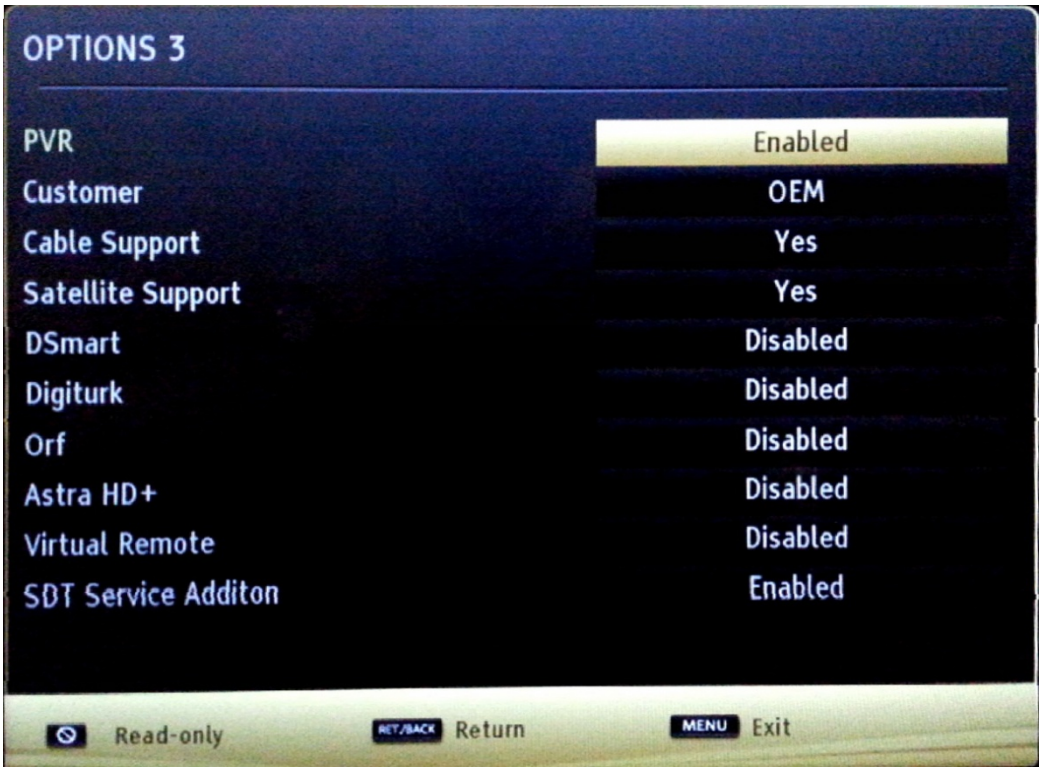
OPTION 1



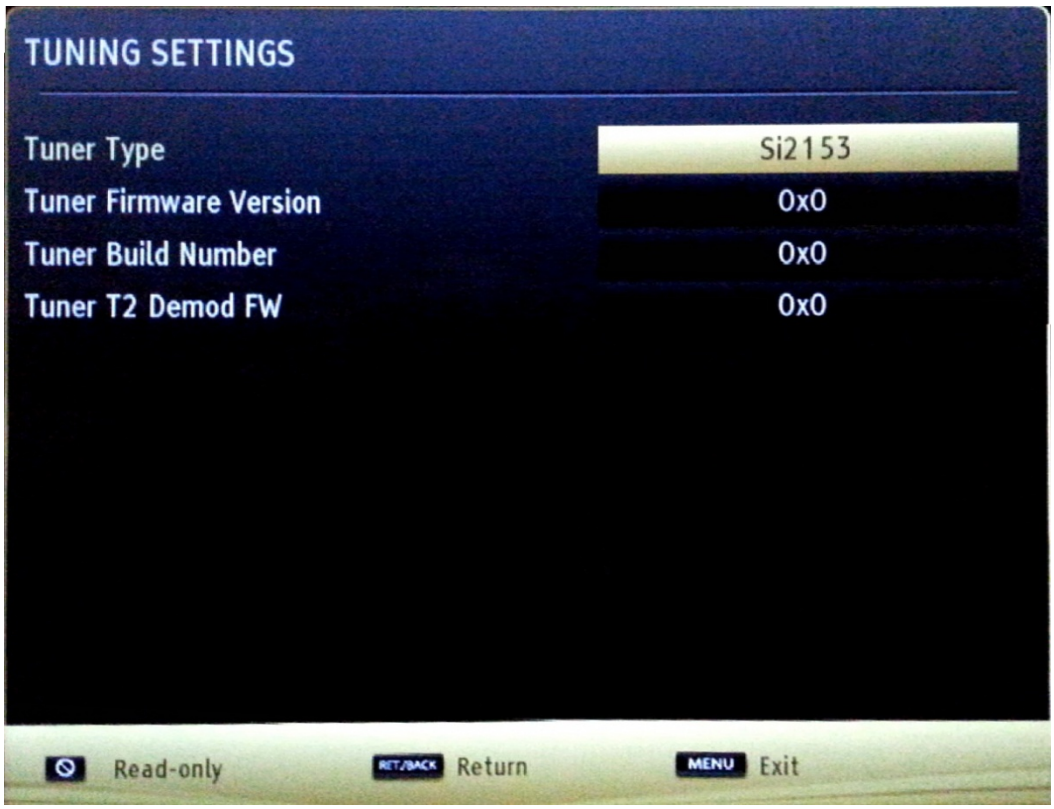
OPTION 2



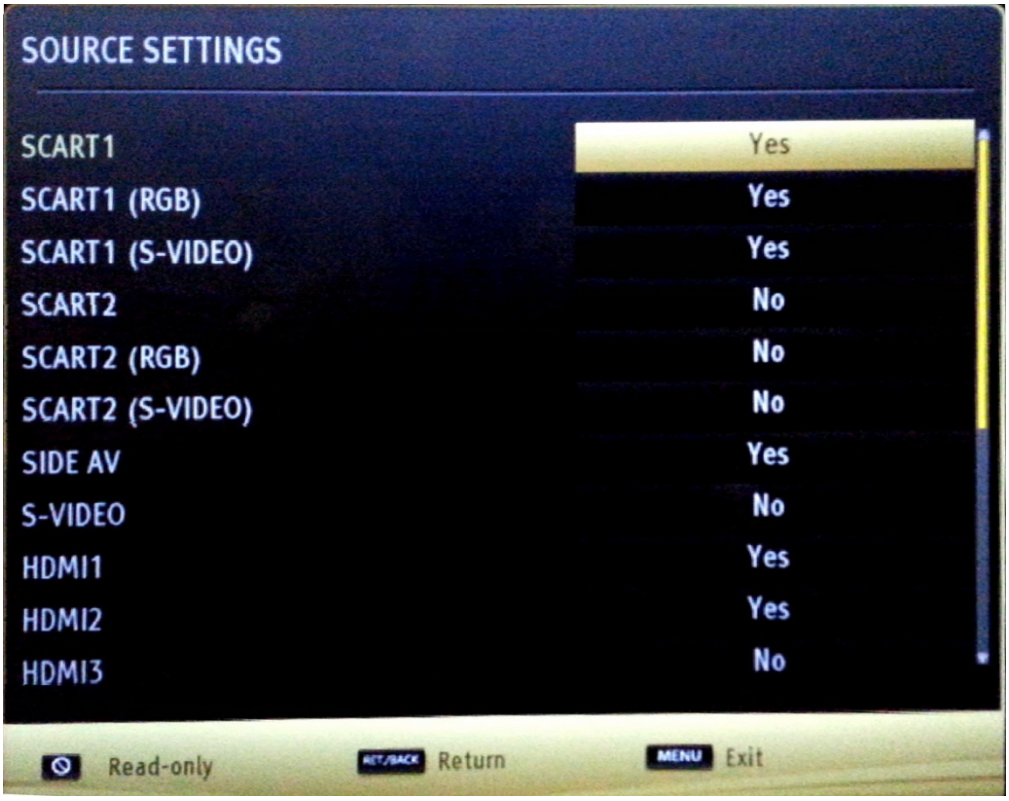
OPTION 3



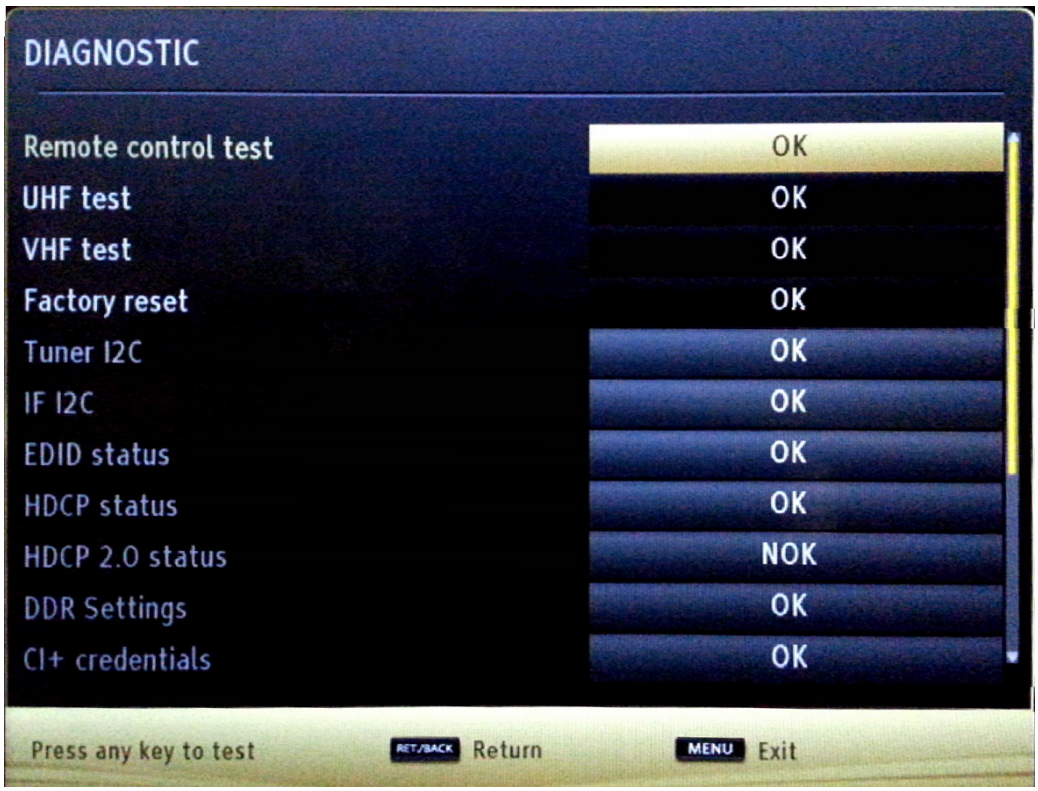
D. TUNNING SETTINGS



E. SOURCE SETTINGS



F. DIAGNOSTIC



G. *USB OPERATIONS*

USB Operations is used for updating panel, audio, video, etc. configuration parameters on the main software. Necessary files should be copied in the USB stick root directory not in a file. In addition, the tool called mksquashfs needs to be copied in the root directory. Below files can be updated;

- ptf.ptf
- PQF.bin
- PCF.pcf
- preset_list.sdx
- AQ.bin
- bornova_hwprofile.bin
- bornova_swprofile.bin
- logo.bin
- hdmiedid.bin
- vgaedid.bin
- PRODUCTION_CREDENTIALS.bin
- hdcpkey.bin

After making ready USB stick contents, plug the stick in to TV and run Usb Operations in one of the two ways, via service menu or running test tool command of "USBOPERATIONS"

The update will be finished within couple of seconds. If everything goes well, you will get following messages in bold format at the uart output,

>>> Update RO success <<<

...

>>> Update ROFIX success <<<

17. SOFTWARE UPDATE

Software update procedure can be done by following these steps below:

1. The format of the USB stick, which will be used in software update, should be in FAT32.
2. “bornova_usb_update.bin” and “bornova_usb_update.scr” files should be copied in the root directory.
3. Plug in USB stick to the TV when it is powered off.
4. Press and hold the “OK” button in the remote controller while the TV is turned off then turn on the TV. When IR LED starts to blink, release the “OK” button and wait for installation. It may take several minutes.

This procedure finishes successfully with First Time Installation screen and then required selections will be done

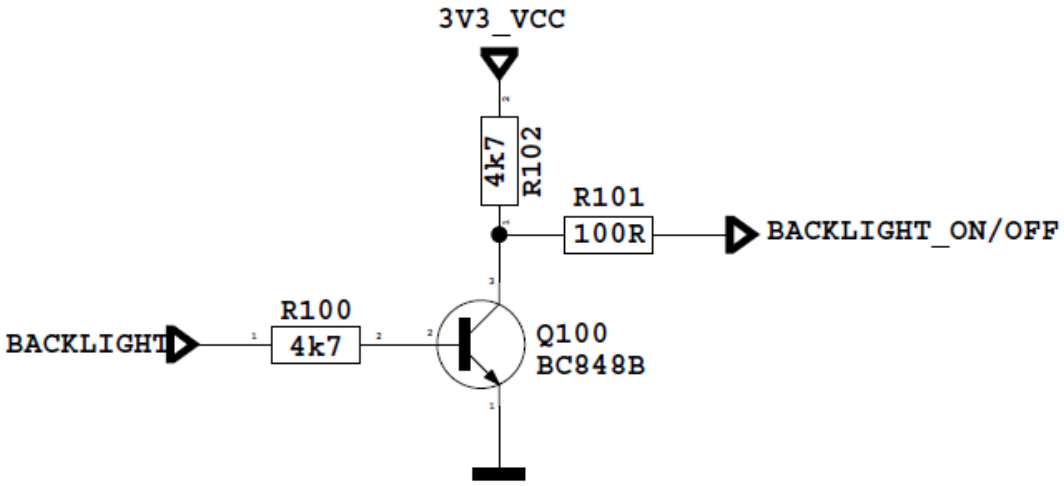
18. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

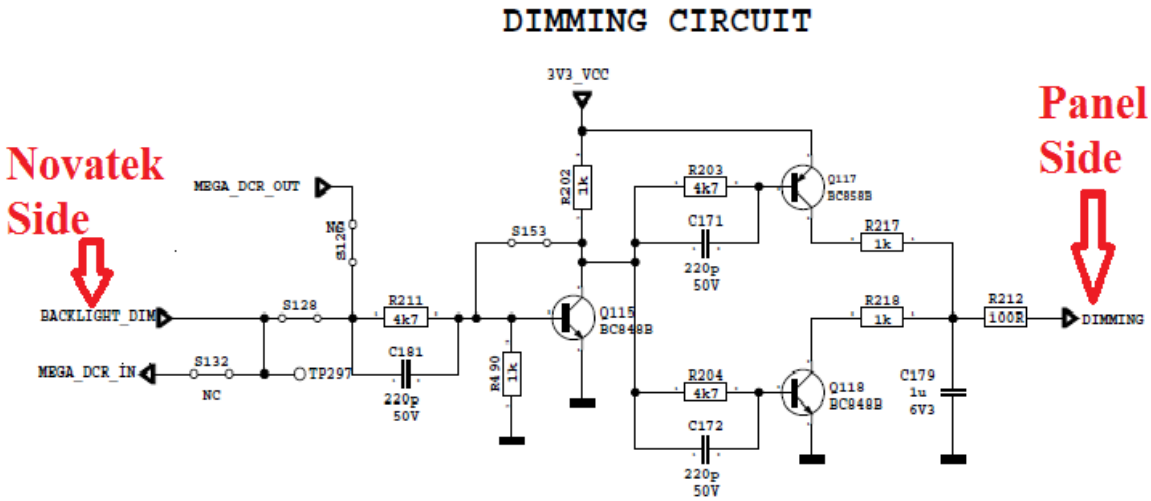
Problem: TV is working, IR led is OFF but there is no picture and backlight on the panel.

Possible causes: BACKLIGHT_ON/OFF pin, DIMMING pin, backlight supply, STBY ON/OFF pin

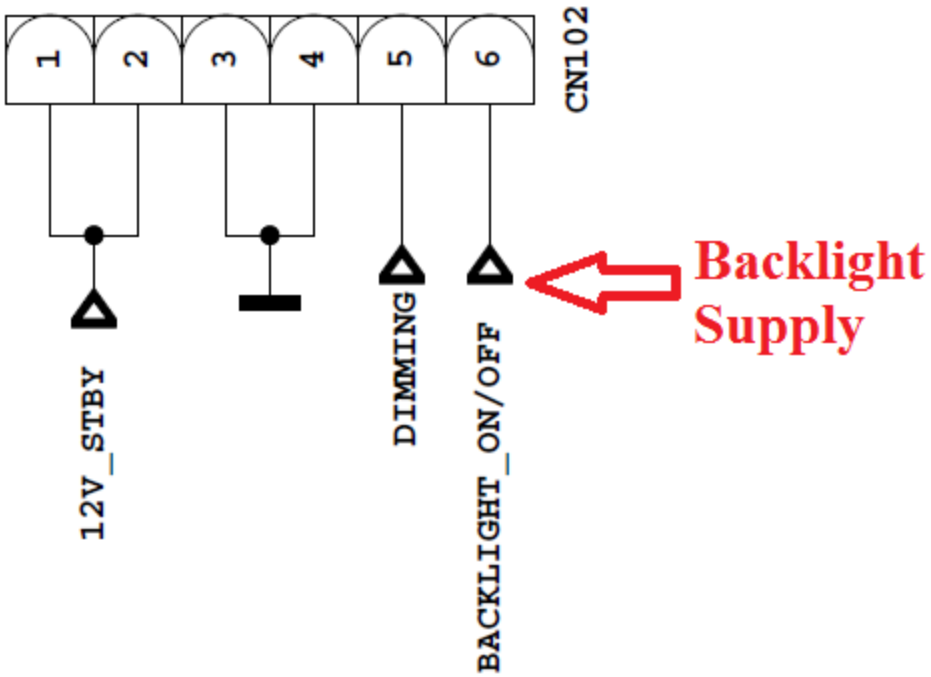
Solution: BACKLIGHT_ON/OFF pin should be high in backlight open position. If it is low, please check Q100 and panel cables.



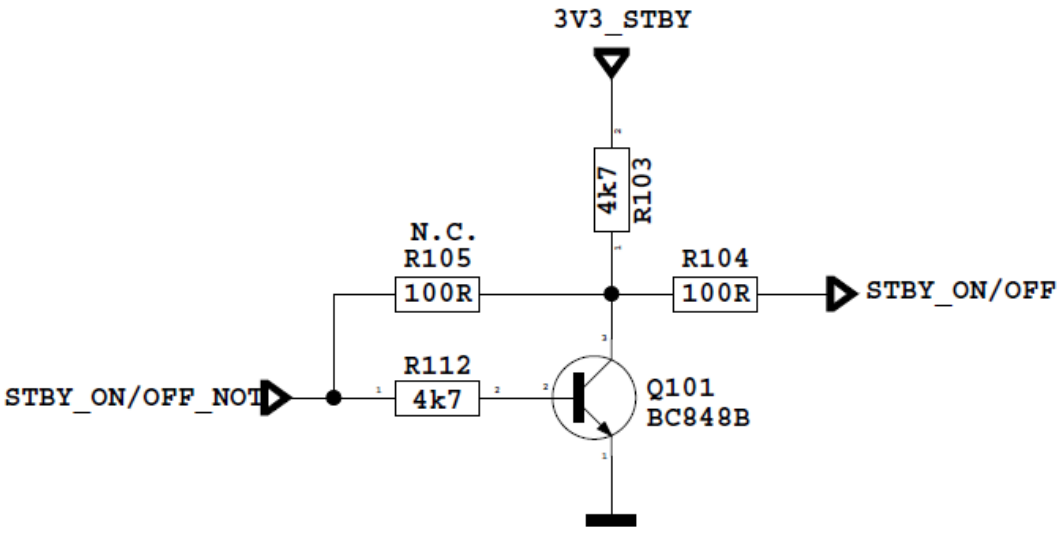
DIMMING pin should be high or square wave in backlight open position. If it is low, please check S128 for Novatek side and panel or power cables, connectors.



For W/ADAPTOR models, backlight power supply should be in panel specs. Please check CN102 and related connectors for power supply cards.



STBY_ON/OFF should be low for standby on condition, please check R104.

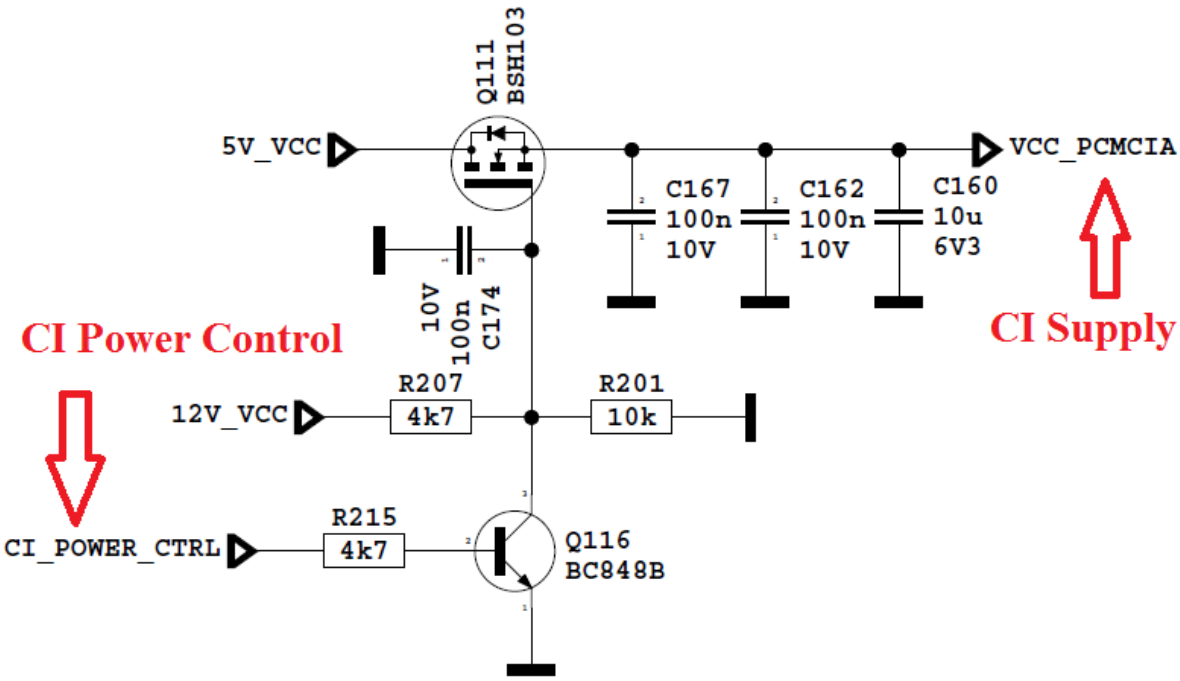


B. *CI MODULE PROBLEM*

Problem: CI is not working when CI module inserted.

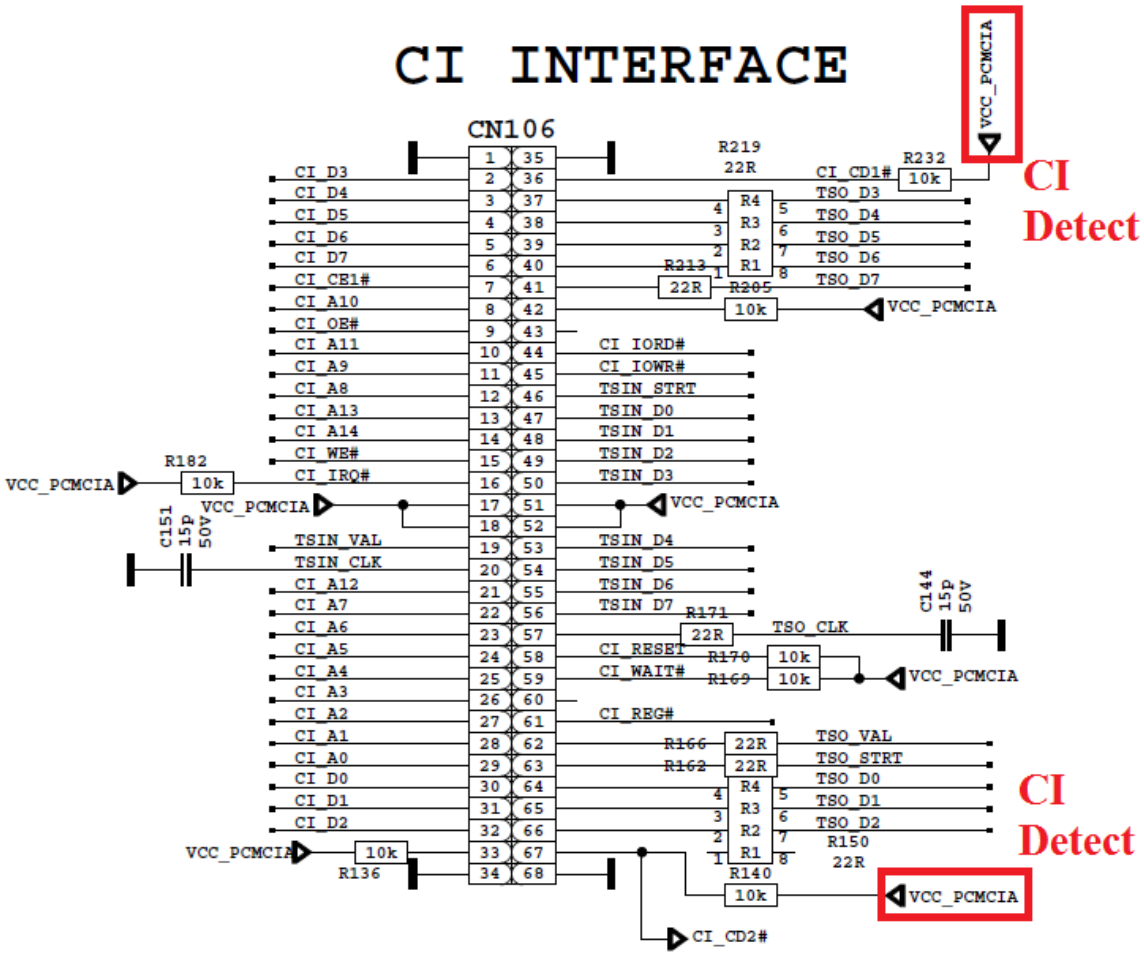
Possible causes: Supply, supply control pin, detect pins, mechanical positions (short circuit) of pins.

Solution: CI supply should be 5V when CI module inserted. If it is not 5V please check CI_POWER_CTRL, this pin should be low.



Please check mechanical positions of CI module in case a short circuit.

Detect ports should be low. If it is not low, please check CI connector pins, CI module pins and VCC_PCMCIA.

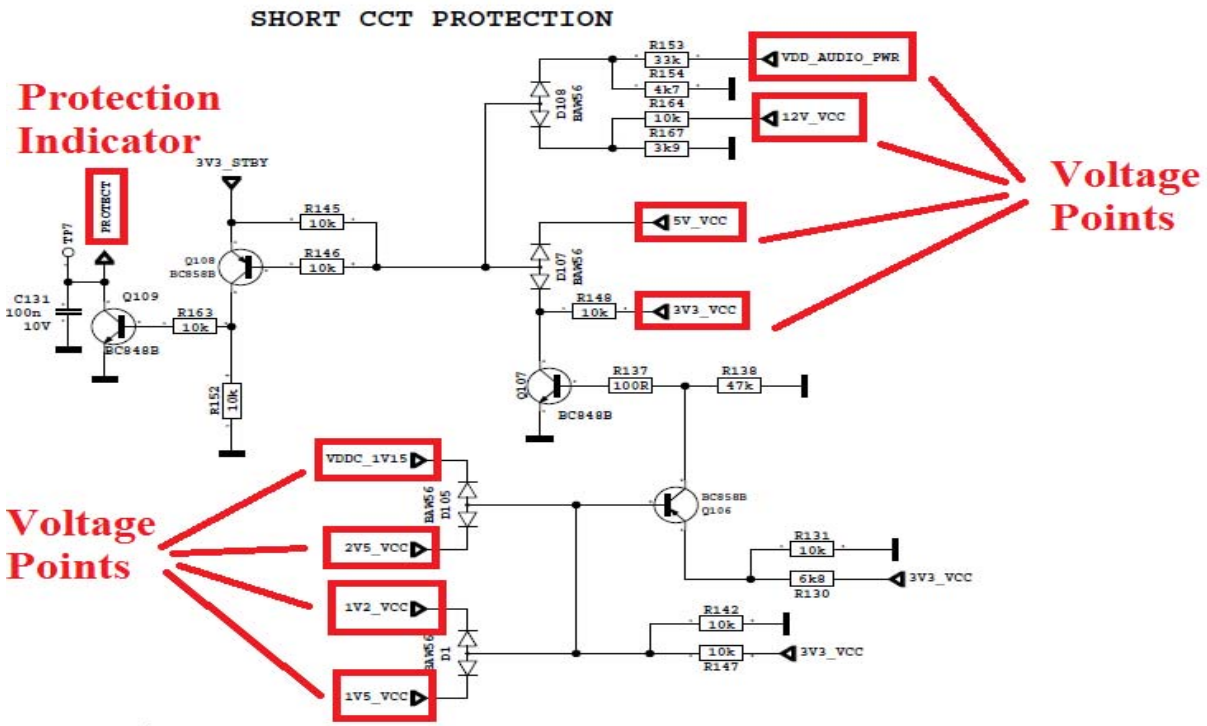


C. ***LED BLINKING PROBLEM***

Problem: LED blinking, no other operation

Possible causes: A short circuit on Vcc voltages.

Solution: Protect pin should be logic high while the TV is in normal operation. When there is a short circuit, protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.

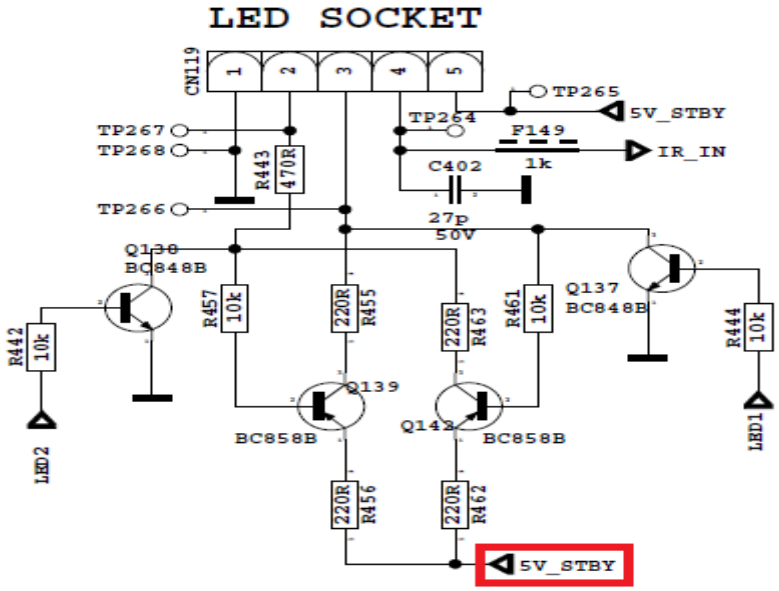


D. ***IR PROBLEM***

Problem: IR or LED is not working.

Possible causes: No supply on the LED card.

Solution: Please check LED card supply.

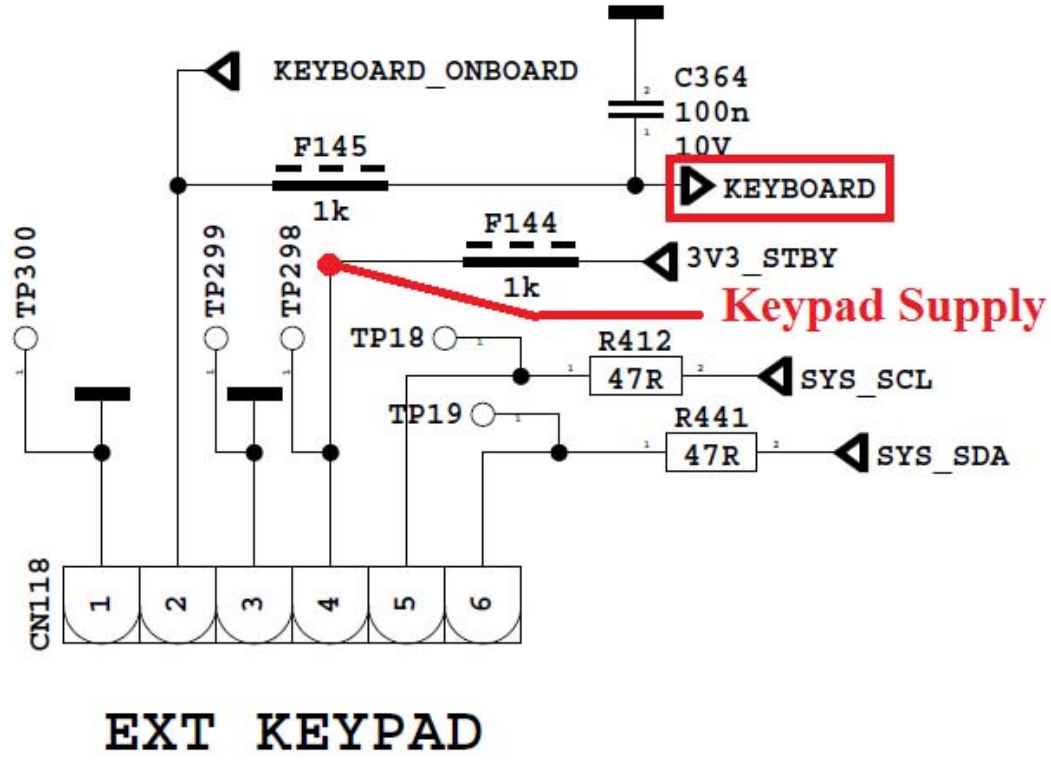


E. KEYPAD OR TOUCHPAD PROBLEM

Problem: Keypad or Touchpad is not working.

Possible causes: No supply on the Keypad card.

Solution: Please check Keypad supply and KEYBOARD pin.

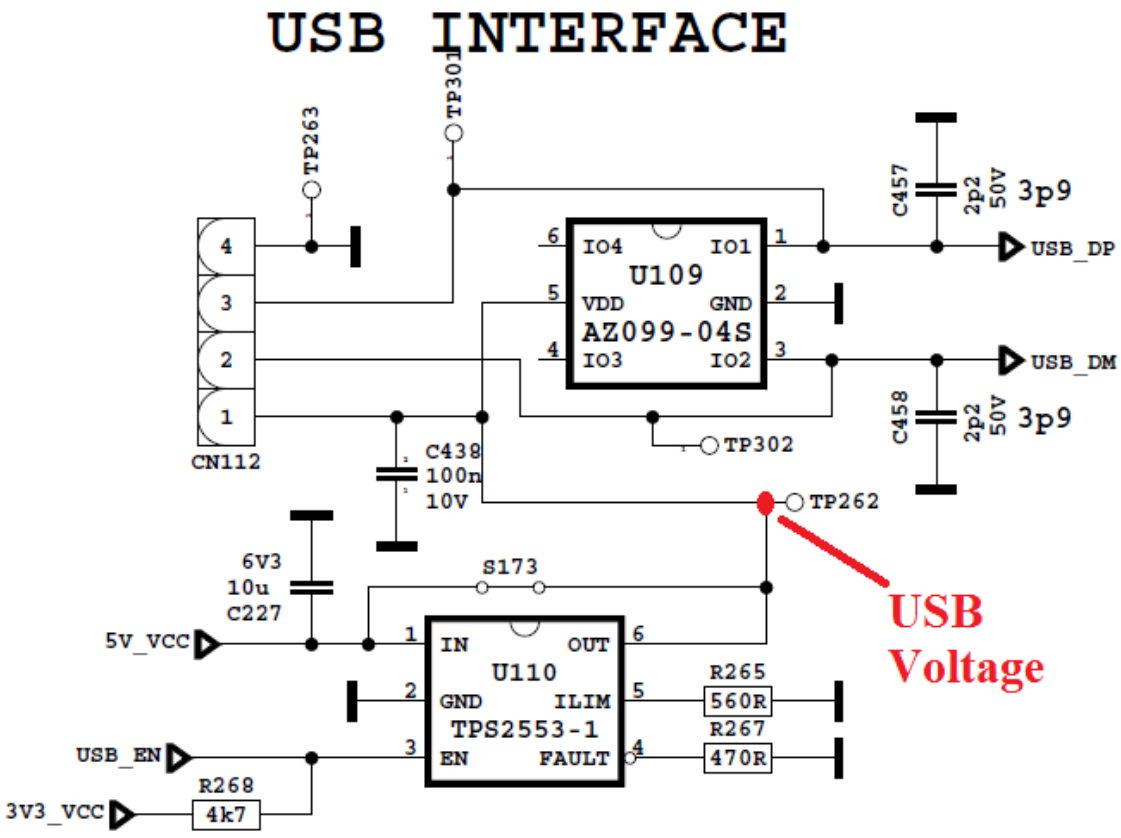


F. *USB PROBLEMS*

Problem: USB is not working or no USB Detection.

Possible causes: No supply on the USB Interface circuit.

Solution: Please check USB Supply, it should be nearly 5V.

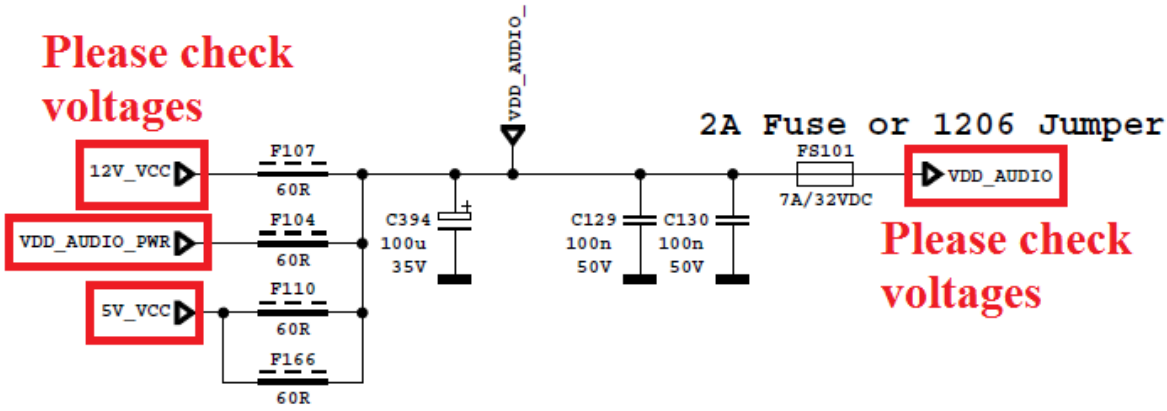


G. *NO SOUND PROBLEM AT MAIN SPEAKERS*

Problem: No audio at main speaker outputs.

Possible causes: No supply voltages on VDD_AUDIO, 5V_VCC, 3V3_VCC, 12V_VCC or VDD_AUDIO_PWR. A problem in headphone connector or headphone detect circuit.

Solution: Please check supply voltages of VDD_AUDIO, 5V_VCC, 3V3_VCC, 12V_VCC and VDD_AUDIO_PWR with a voltage-meter. Please check headphone connector and headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.

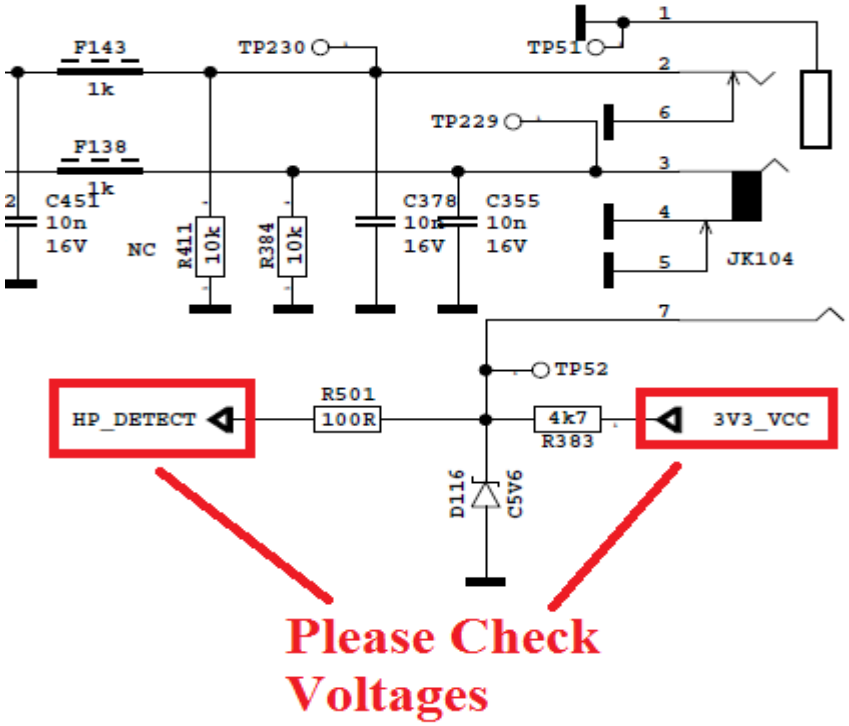


H. NO SOUND PROBLEM AT HEADPHONE

Problem: No audio at headphone output.

Possible causes: No supply voltages on 5V_VCC, 3V3_VCC or a problem in headphone connector or headphone detect pin.

Solution: Please check supply voltages of 5V_VCC, 3V3_VCC with a voltage-meter. Please check headphone connector and headphone detect pin when the headphone is plugged in. Measure voltage at HP_DETECT pin, it should be low state (0V). A headphone sign should be seen in OSD screen when volume up or down button is pressed in the remote controller.



İ. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

Possible causes: No power supply or a problem about software.

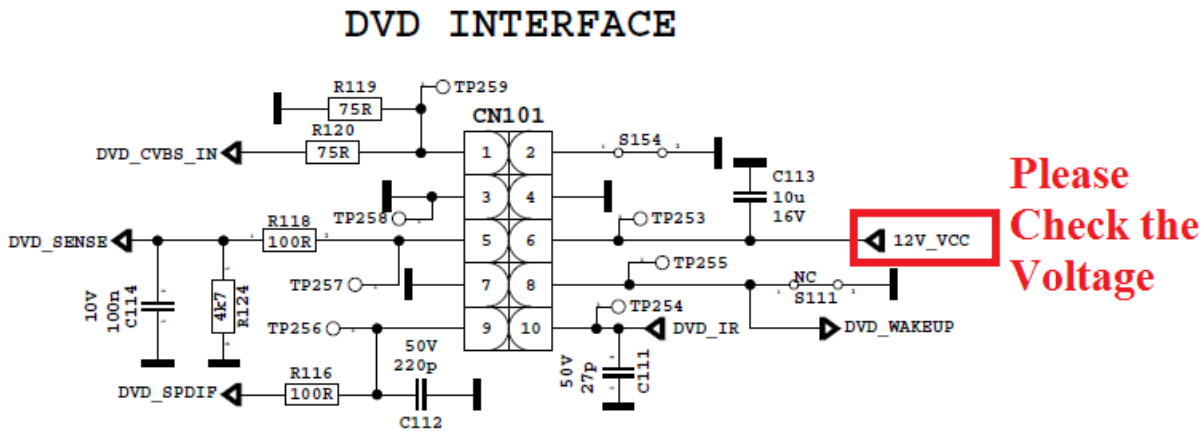
Solution: Please check 12V_VCC, 5V_VCC and 3V3_VCC with a voltage-meter. Try to update TV with latest SW. Additionally it is good to check SW printouts via hyper-terminal (or TeraTerm). These printouts may give a clue about the problem.

J. DVD PROBLEM

Problem: DVD is not working.

Possible causes: A problem in Service menu or no DVD supply voltage.

Solution: Please check that DVD source is selected in Service menu. Please check supply voltage of DVD namely 12V_VCC.

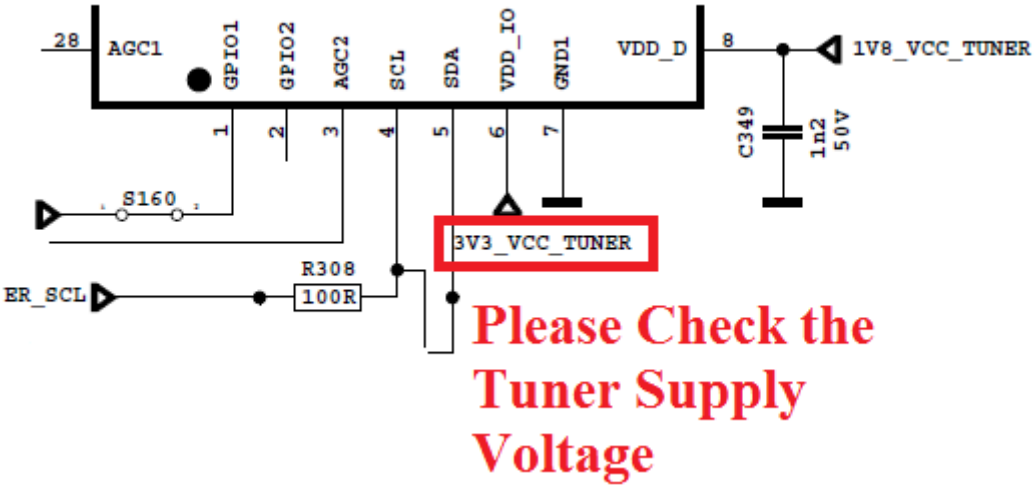


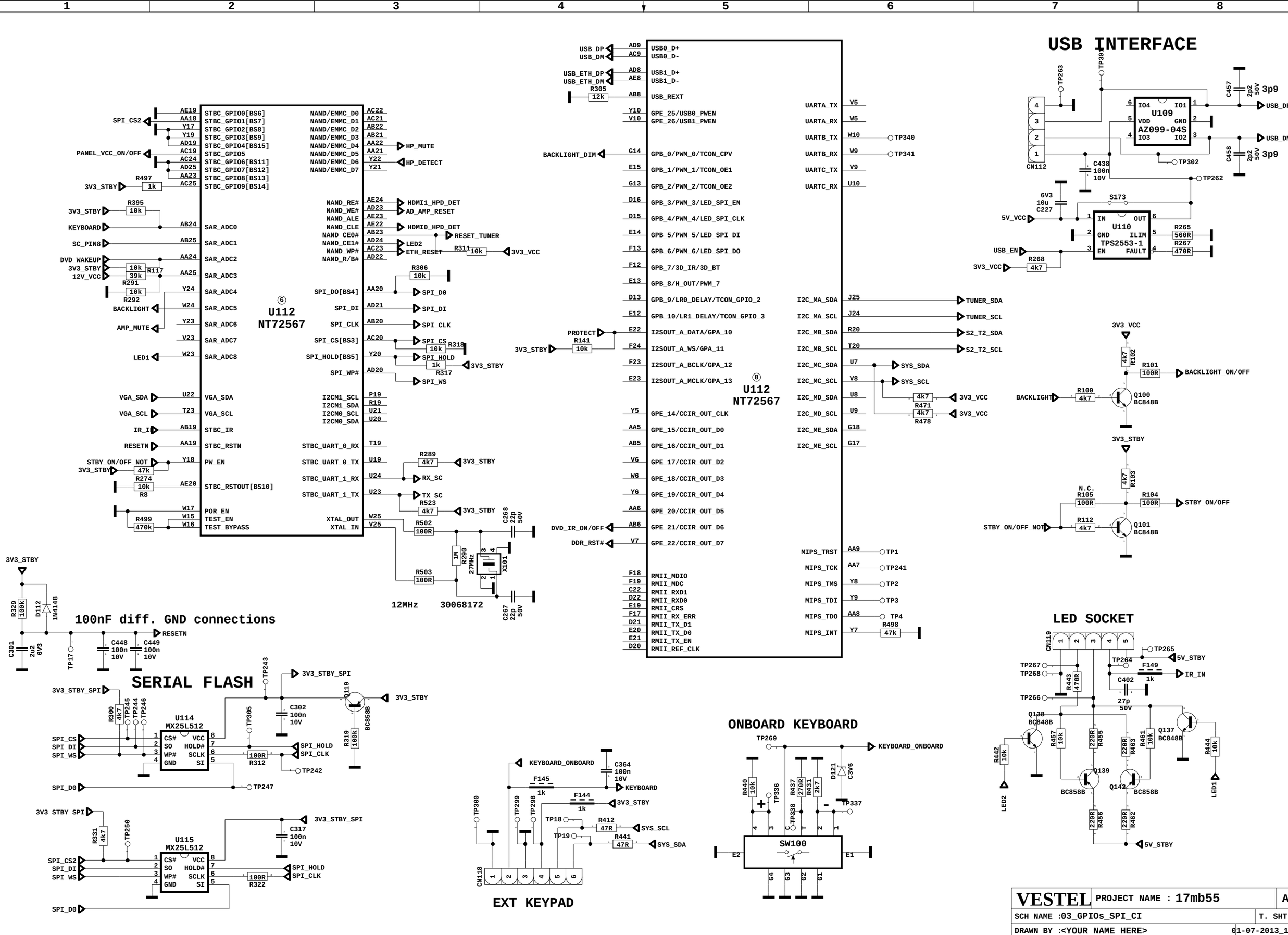
K. NO SIGNAL PROBLEM

Problem: No signal in TV mode.

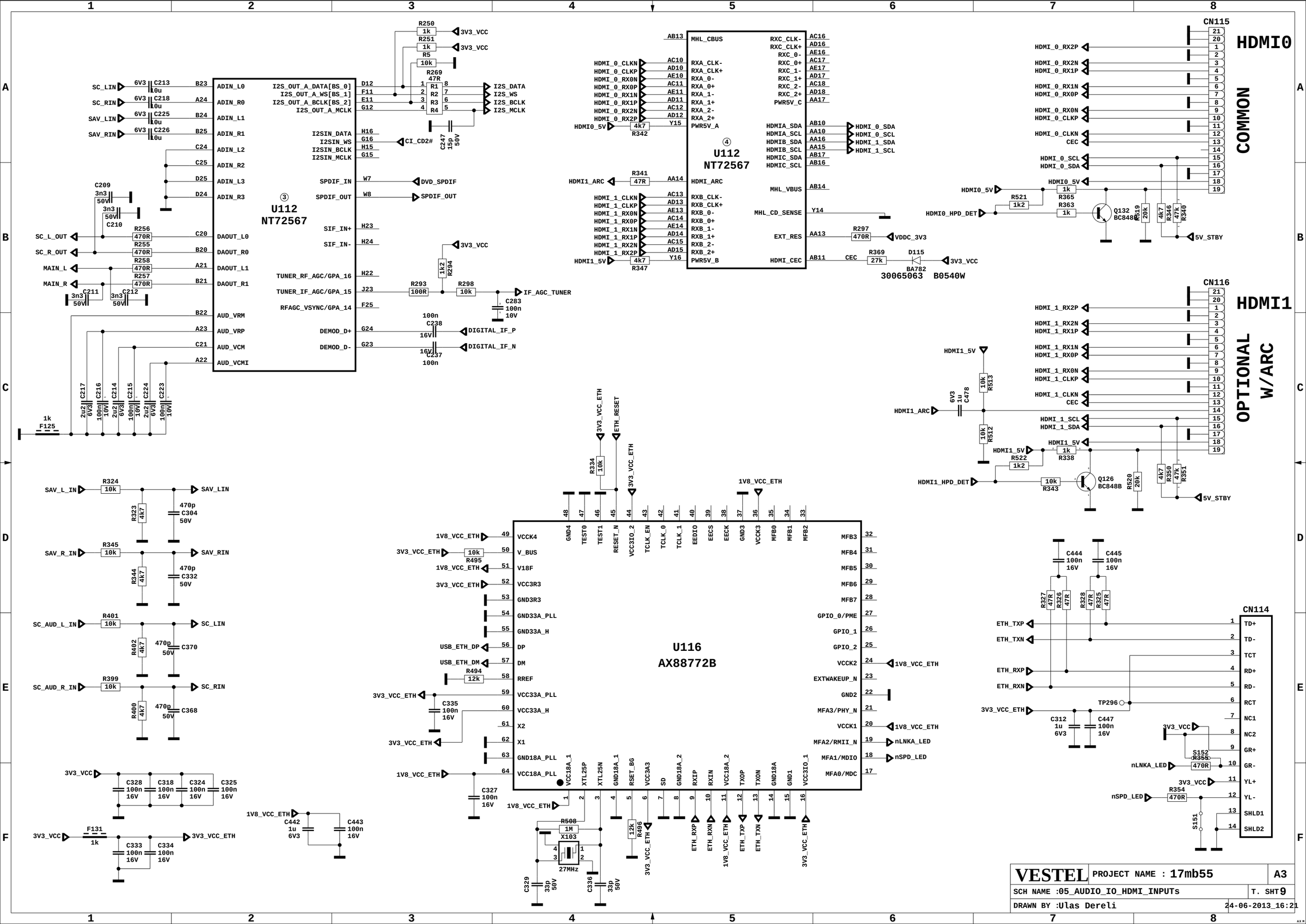
Possible causes: A problem in Service menu or no tuner supply voltage.

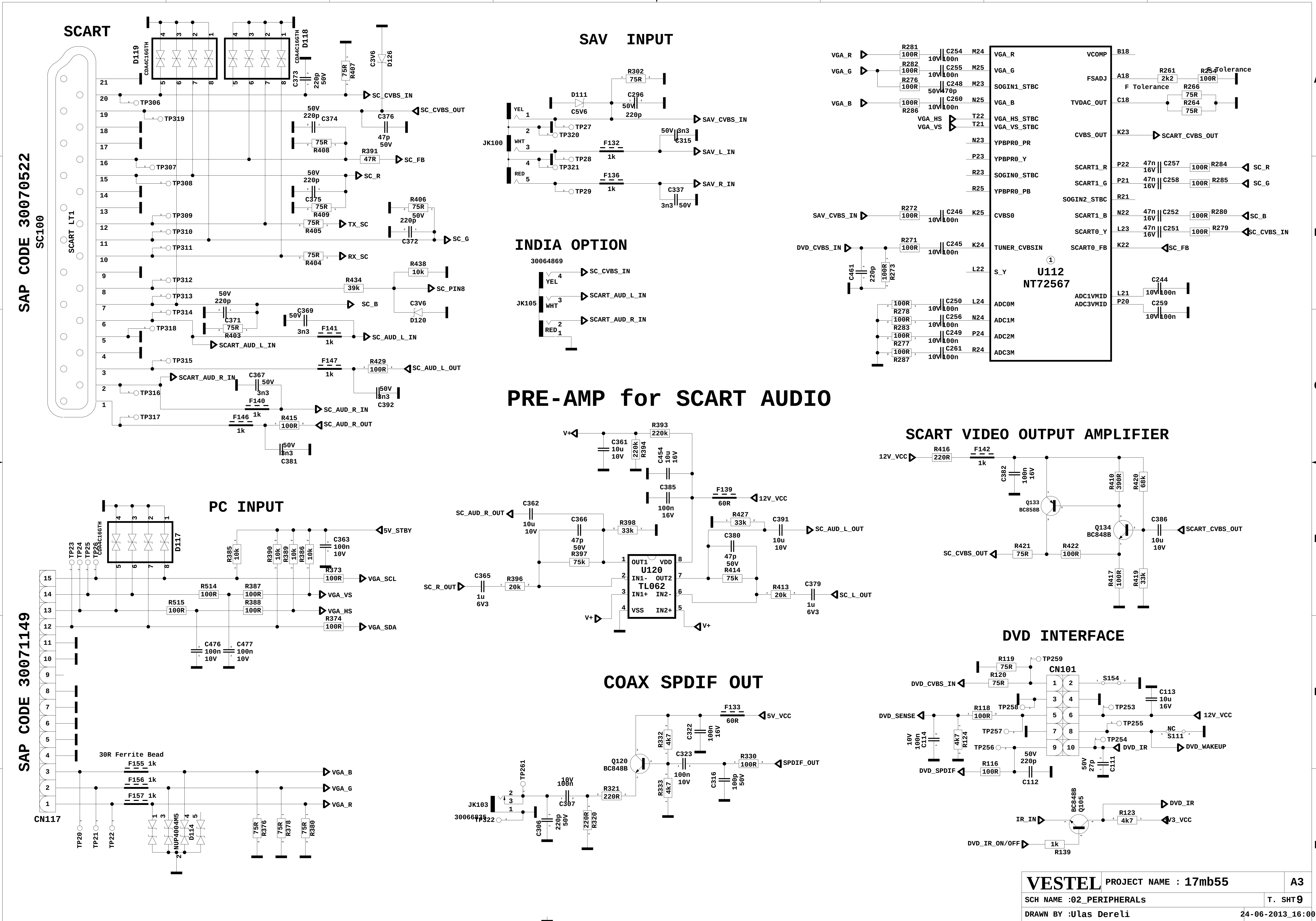
Solution: Please check tuner supply voltage; 3V3_TUN. Check tuner options are correctly set in Service menu. Check AGC voltage at IF_AGC pin of tuner, it should be more than 2V.

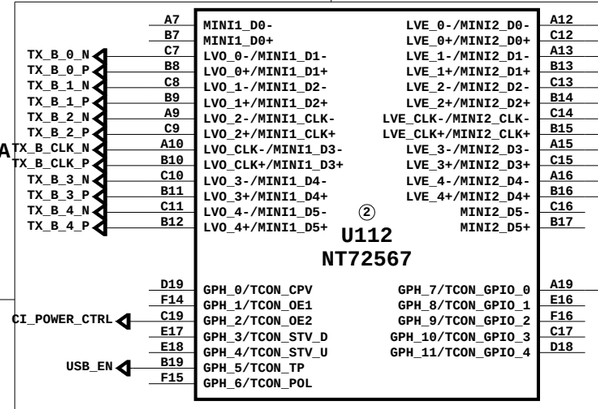


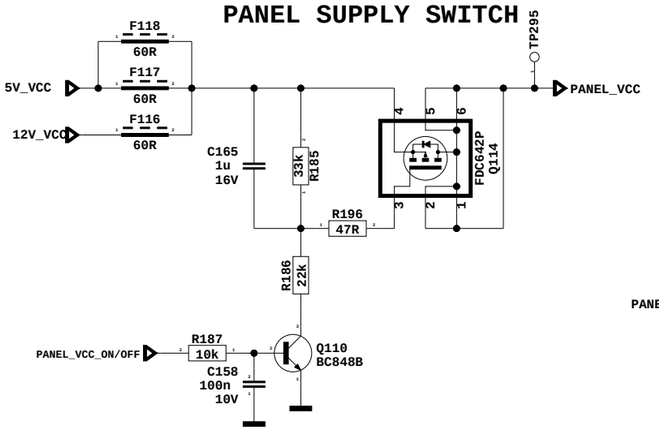


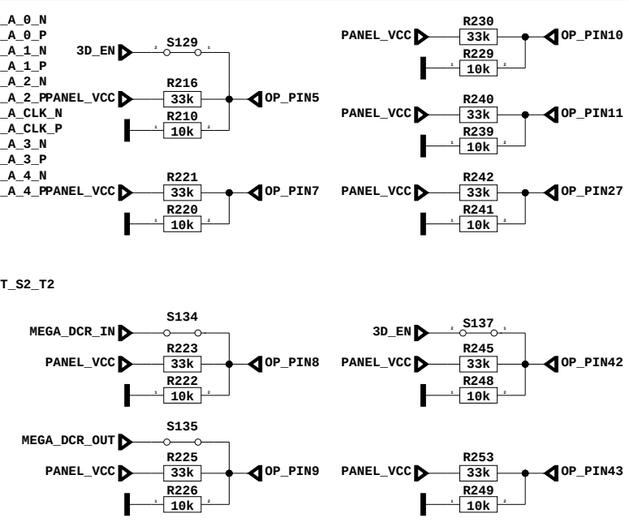
VESTEL	PROJECT NAME : 17mb55	A3
SCH NAME :03_GPIOs_SPI_CI		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		01-07-2013_13:59

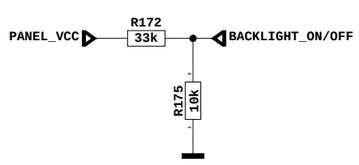

U112
NT72567
ADIN_L0
ADIN_R0
ADIN_L1
ADIN_R1
ADIN_L2
ADIN_R2
ADIN_L3
ADIN_R3
DAOUT_L0
DAOUT_R0
DAOUT_L1
DAOUT_R1
AUD_VRM
AUD_VRP
AUD_VCM
AUD_VCMI
I2S_OUT_A_DATA[BS_0]
I2S_OUT_A_WS[BS_1]
I2S_OUT_A_BCLK[BS_2]
I2S_OUT_A_MCLK
I2SIN_DATA
I2SIN_WS
I2SIN_BCLK
I2SIN_MCLK
SPDIF_IN
SPDIF_OUT
SIF_IN+
SIF_IN-
TUNER_RF_AGC/GPA_16
TUNER_IF_AGC/GPA_15
RFAGC_VSYNC/GPA_14
DEMOD_D+
DEMOD_D-
SC_LIN
SC_RIN
SAV_LIN
SAV_RIN
SC_L_OUT
SC_R_OUT
MAIN_L
MAIN_R
I2S_DATA
I2S_WS
I2S_BCLK
I2S_MCLK
CI_CD2#
DVD_SPDIF
SPDIF_OUT
IF_AGC_TUNER
DIGITAL_IF_P
DIGITAL_IF_N
3V3_VCC
F125
F131
U112
NT72567
MHL_CBUS
RXA_CLK-
RXA_CLK+
RXA_0-
RXA_0+
RXA_1-
RXA_1+
RXA_2-
RXA_2+
PWR5V_A
HDMI_ARC
RXB_CLK-
RXB_CLK+
RXB_0-
RXB_0+
RXB_1-
RXB_1+
RXB_2-
RXB_2+
PWR5V_B
RXC_CLK-
RXC_CLK+
RXC_0-
RXC_0+
RXC_1-
RXC_1+
RXC_2-
RXC_2+
PWR5V_C
HDMIA_SDA
HDMIA_SCL
HDMIB_SDA
HDMIB_SCL
HDMIC_SDA
HDMIC_SCL
MHL_VBUS
MHL_CD_SENSE
EXT_RES
HDMI_CEC
HDMI_0_SDA
HDMI_0_SCL
HDMI_1_SDA
HDMI_1_SCL
VDDC_3V3
HDMI0_5V
HDMI1_ARC
HDMI1_5V
CN115
HDMI0
COMMON
HDMI_0_RX2P
HDMI_0_RX2N
HDMI_0_RX1P
HDMI_0_RX1N
HDMI_0_RX0P
HDMI_0_RX0N
HDMI_0_CLKP
HDMI_0_CLKN
CEC
HDMI_0_SCL
HDMI_0_SDA
HDMI0_HPD_DET
5V_STBY
Q132
BC848B
CN116
HDMI1
OPTIONAL
W/ARC
HDMI_1_RX2P
HDMI_1_RX2N
HDMI_1_RX1P
HDMI_1_RX1N
HDMI_1_RX0P
HDMI_1_RX0N
HDMI_1_CLKP
HDMI_1_CLKN
CEC
HDMI_1_SCL
HDMI_1_SDA
HDMI1_HPD_DET
Q126
BC848B
5V_STBY
30065063 B0540W
U116
AX88772B
GND4
TEST0
TEST1
RESET_N
VCC3IO_2
TCLK_EN
TCLK_0
TCLK_1
EEDIO
EECS
EECK
GND3
VCCK3
MFB0
MFB1
MFB2
VCCK4
V_BUS
V18F
VCC3R3
GND3R3
GND33A_PLL
GND33A_H
DP
DM
RREF
VCC33A_PLL
VCC33A_H
X2
X1
GND18A_PLL
VCC18A_PLL
MFB3
MFB4
MFB5
MFB6
MFB7
GPIO_0/PME
GPIO_1
GPIO_2
VCCK2
EXTWAKEUP_N
GND2
MFA3/PHY_N
VCCK1
MFA2/RMII_N
MFA1/MDIO
MFA0/MDC
VCC18A_1
XTL25P
XTL25N
GND18A_1
RSET_BG
VCC3A3
SD
GND18A_2
RXIP
RXIN
VCC18A_2
TXOP
TXON
GND18A
GND1
VCC3IO_1
3V3_VCC_ETH
1V8_VCC_ETH
ETH_RESET
X103
27MHz
ETH_RXP
ETH_RXN
ETH_TXP
ETH_TXN
nLNKA_LED
nSPD_LED
CN114
TD+
TD-
TCT
RD+
RD-
RCT
NC1
NC2
GR+
GR-
YL+
YL-
SHLD1
SHLD2
TP296
S152
S151
VESTEL
PROJECT NAME : 17mb55
A3
SCH NAME :05_AUDIO_IO_HDMI_INPUTs
T. SHT 9
DRAWN BY :Ulas Dereli
24-06-2013_16:21

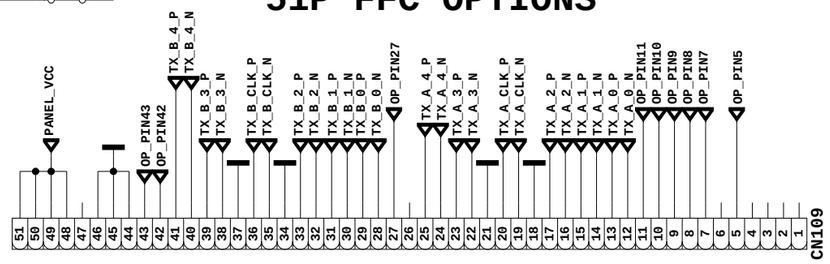

SCART
SAP CODE 30070522
SC100
SCART LT1
SAV INPUT
JK100
INDIA OPTION
30064869
JK105
PRE-AMP for SCART AUDIO
U120
TL062
SCART VIDEO OUTPUT AMPLIFIER
PC INPUT
SAP CODE 30071149
CN117
30R Ferrite Bead
COAX SPDIF OUT
JK103
30066835
DVD INTERFACE
CN101
U112
NT72567
VESTEL
PROJECT NAME : 17mb55
A3
SCH NAME :02_PERIPHERALS
T. SHT9
DRAWN BY :Ulas Dereli
24-06-2013_16:00

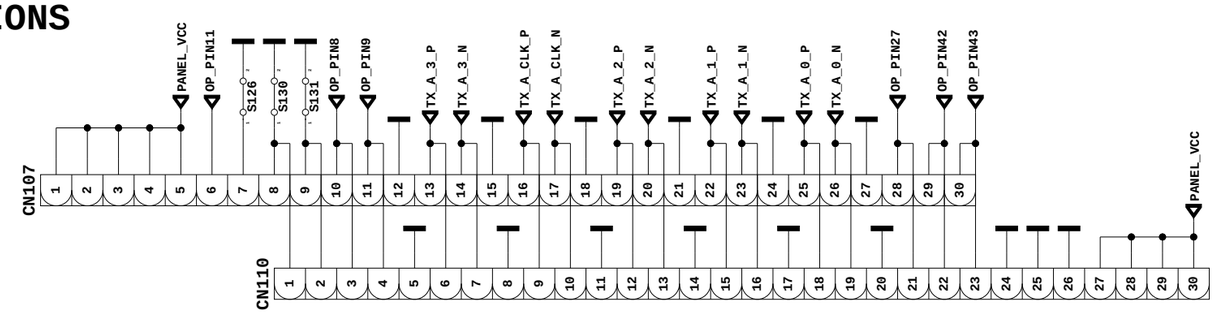


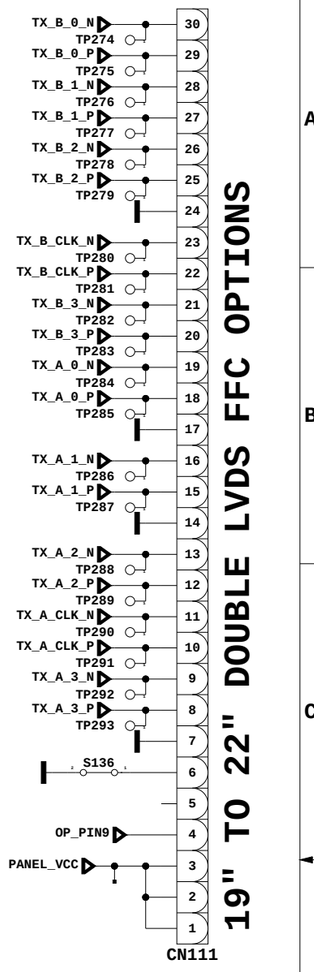


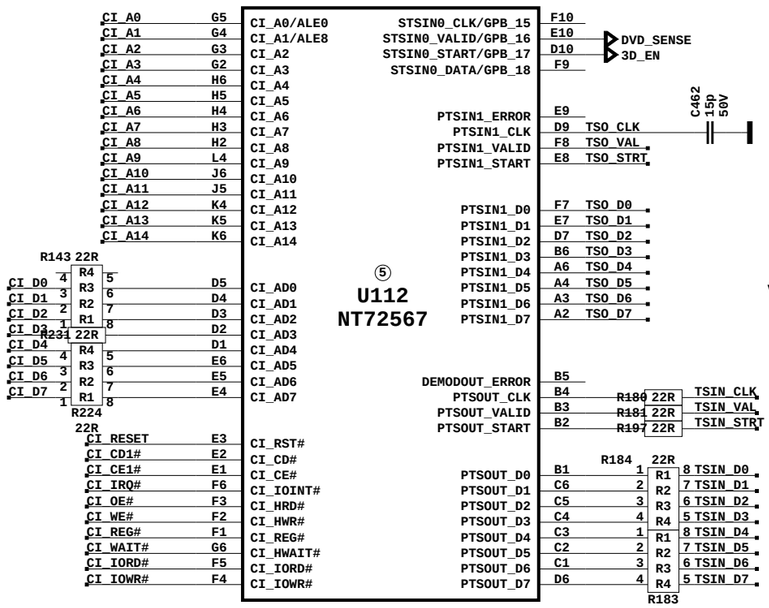


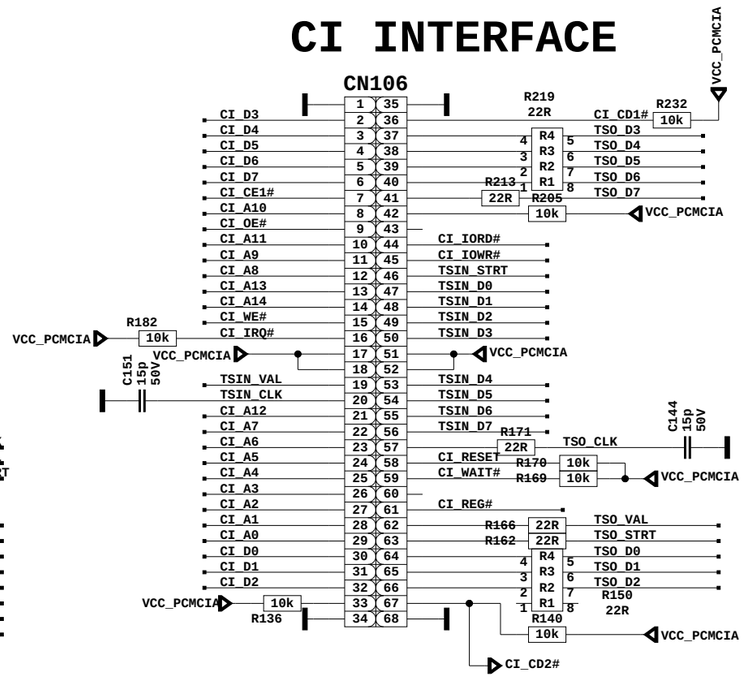


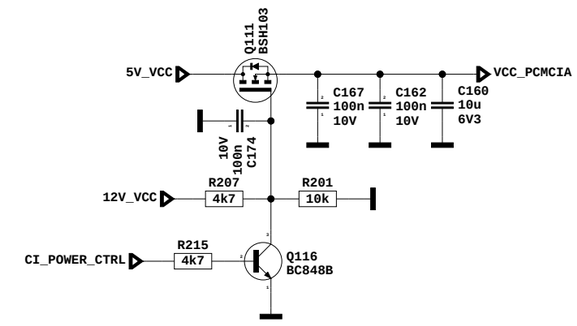






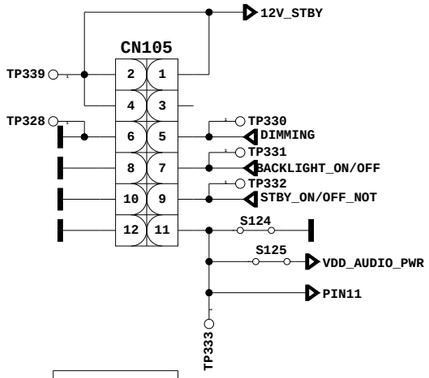






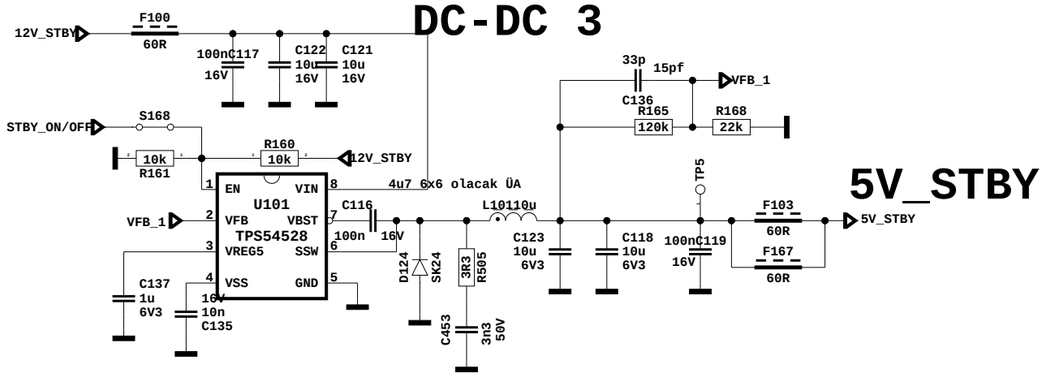
VESTEL	PROJECT NAME : 17mb55	A3
SCH NAME :07_USB_LVDS_OUT		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		02-07-2013_09:26

W/B2CABLE

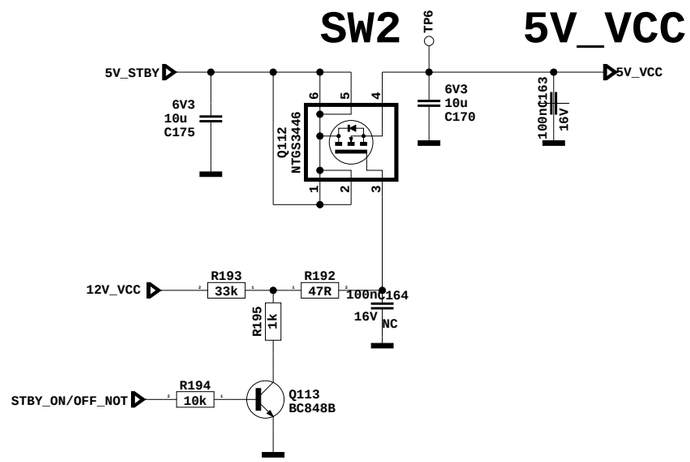


W/B2B

DC-DC 3

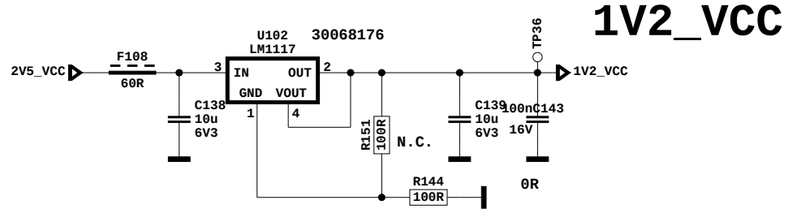


W/ADAPTOR

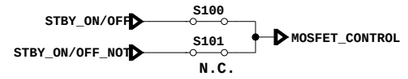


W/S2 W/T2

LDO2

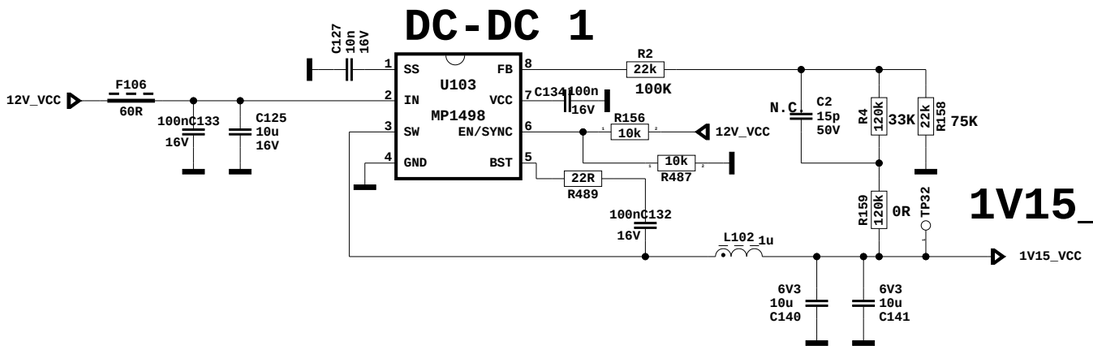


1V2_VCC

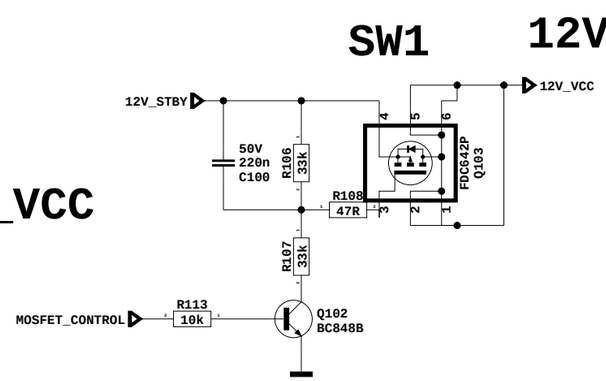


COMMON

DC-DC 1



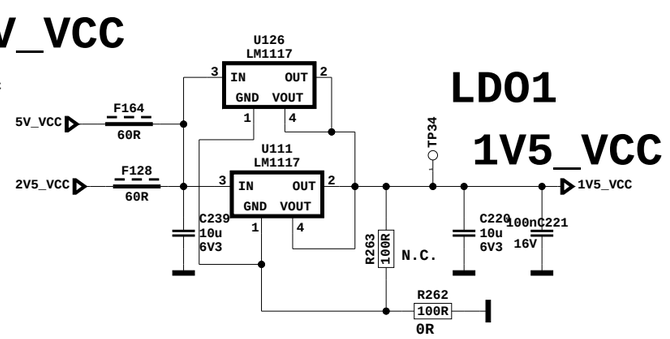
SW1



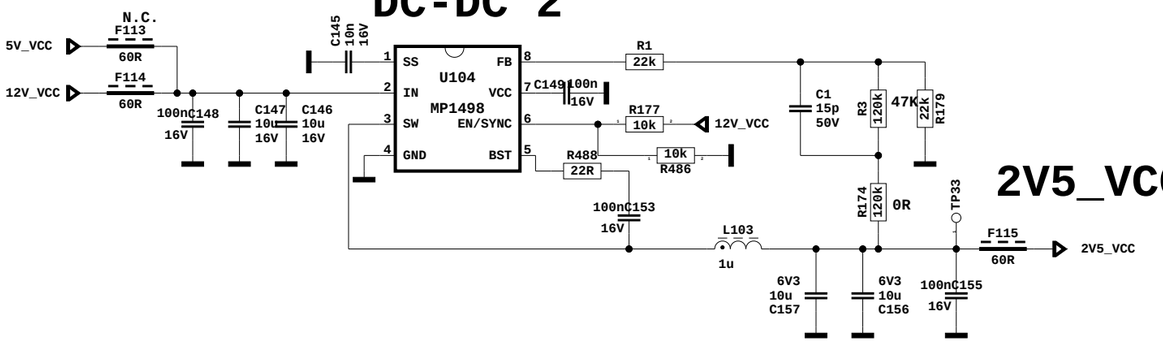
12V_VCC

LDO1

1V5_VCC

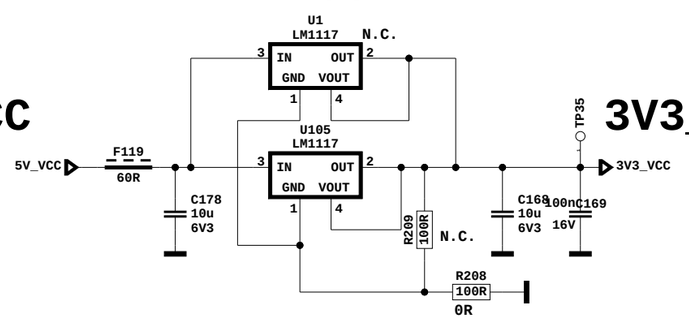


DC-DC 2



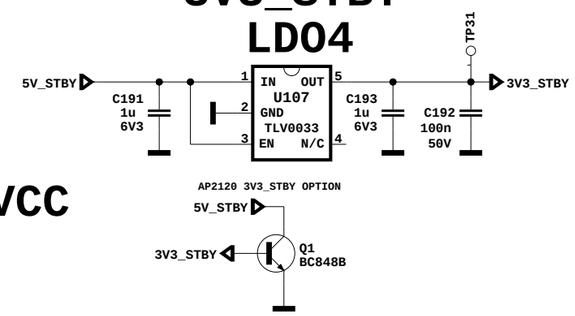
2V5_VCC

LDO3



3V3_VCC

3V3_STBY
LDO4



VESTEL	PROJECT NAME : 17mb55	A3
SCH NAME :08_POWER		T. SHT 9
DRAWN BY :Ulas Dereli		24-06-2013_16:22

I2C ADDR: C0

I2C ADDR: 10

I2C ADDR: 18

I2C ADDR: C8

U119
SI2158

U108
LNBH29EPTR

U118
TPS2553-1

U125
RDA5815S

U106
SI2166

24MHz

3R3
30051799

BC858B 30010731
Q131

PROJECT NAME	17mb55
SCH NAME	01_TUNER_S2_TUNER_DEMOD_LNBP
DRAWN BY	Ulas Dereli
	A3
T. SHT	9
	01-07-2013_13:39

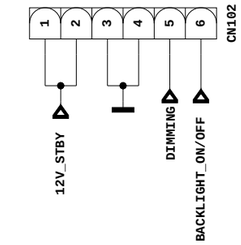
DDR3 RAM

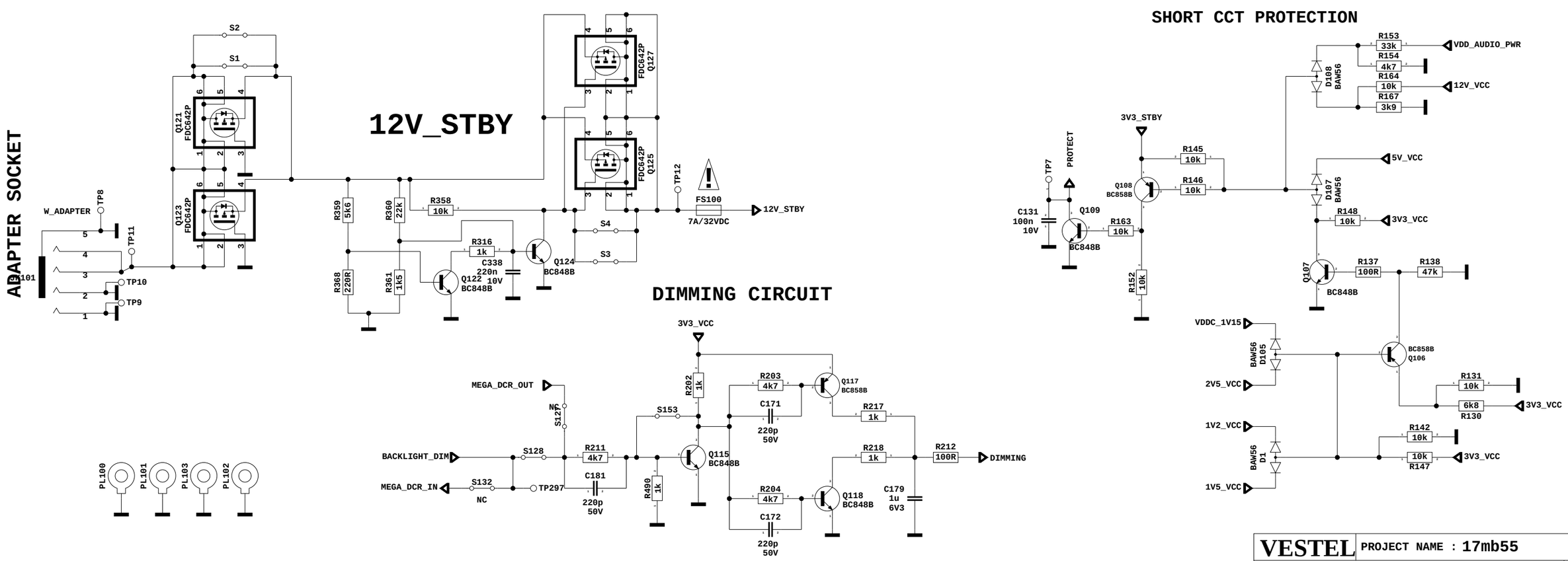
NT72567 U112 ⑨

U112 NT72567 ⑦

U113 H5TQ2G63BFR-PB

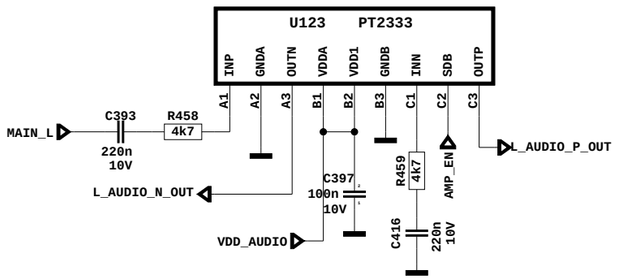
VESTEL	PROJECT NAME : 17mb55	A3
SCH NAME :04_RAM_MAIN_POWER		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		01-07-2013_15:30

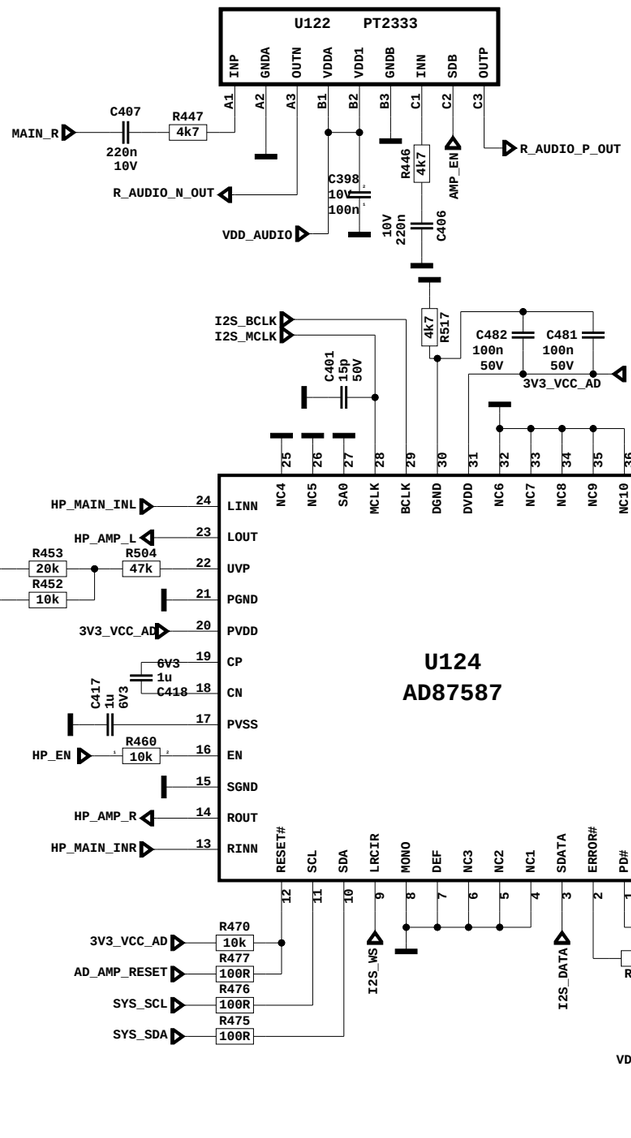




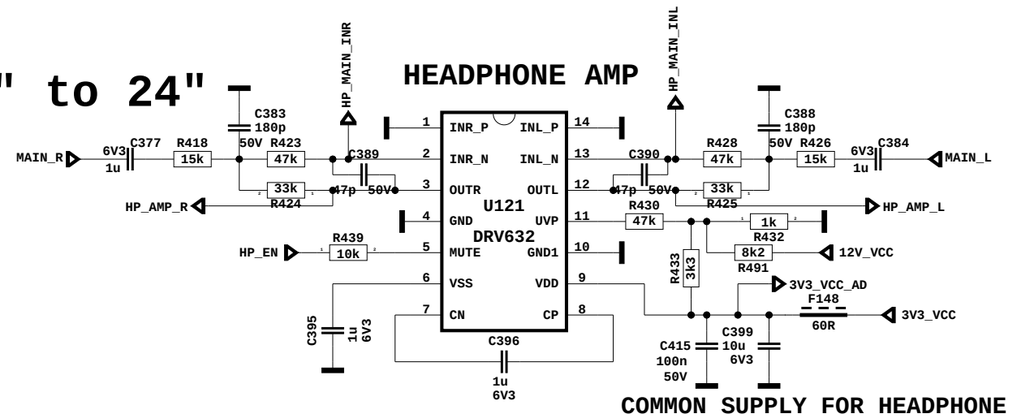
VESTEL	PROJECT NAME : 17mb55		A3
SCH NAME :09_POWER1_CONVERTER		T. SHT	9
DRAWN BY :<YOUR NAME HERE>		24-06-2013_16:02	

AUDIO AMP for 16" to 24"



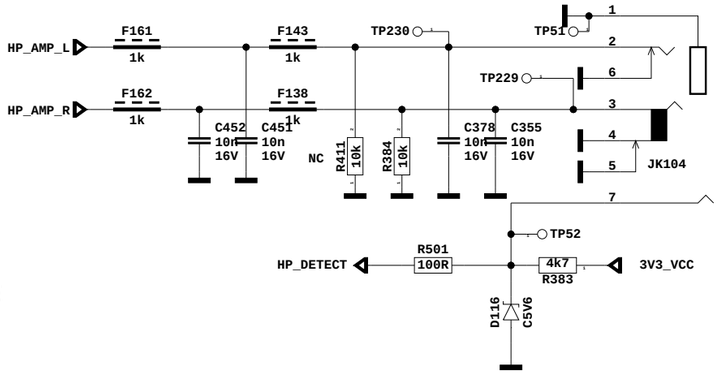


HEADPHONE AMP

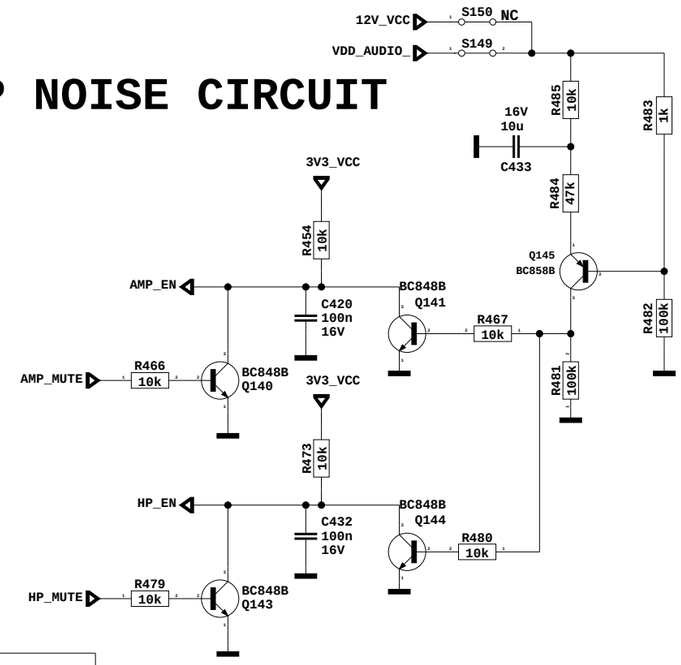


COMMON SUPPLY FOR HEADPHONE

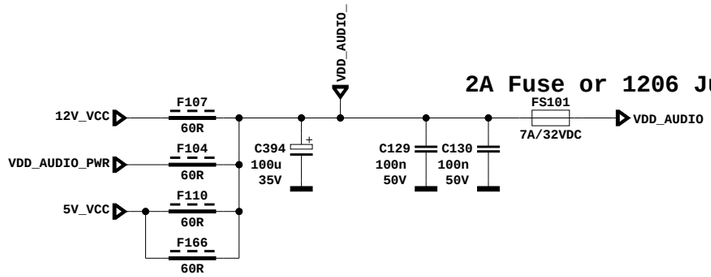
HEADPHONE OUTPUT

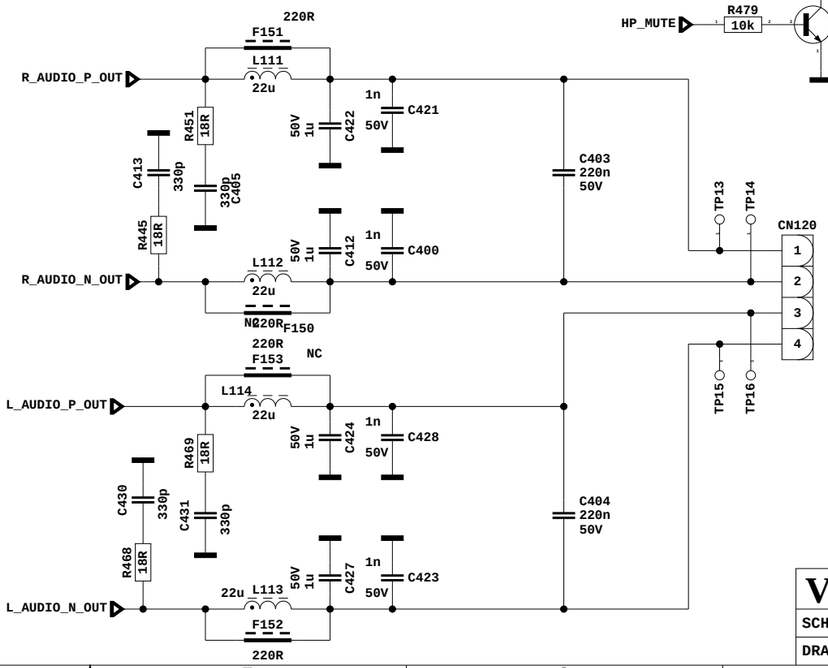


POP NOISE CIRCUIT



2A Fuse or 1206 Jumper





VESTEL	PROJECT NAME : 17mb55	A3
SCH NAME :06_AUDIO_AMP_HP_AMP		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		24-06-2013_16:22